



NSF017120T1A0

1200 V, 17 mΩ, N-channel SiC MOSFET

8 April 2026

Product data sheet

1. General description

The NSF017120T1A0 is a Silicon Carbide based 1200 V power MOSFET in the QDPAK plastic package for surface-mounted, topside-cooled technology. Its excellent R_{DSon} temperature stability, combined with fast switching speed, makes it a product of choice in high power and high voltage industrial applications, such as E-vehicle charging infrastructure, photovoltaic inverters and motor drives.

2. Features and benefits

- Excellent R_{DSon} temperature stability
- Very low switching losses
- Fast reverse recovery
- Fast switching speed
- Temperature independent turn-off switching losses
- Very fast and robust intrinsic body diode
- Faster commutation and improved switching due to the additional Kelvin source pin

3. Applications

- E-vehicle charging infrastructure
- Photovoltaic inverters
- Switch mode power supply
- Uninterruptable power supply
- Motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{DS}	drain-source voltage		-	-	1200	V	
V_{GS}	gate-source voltage		[1]	-10	-	22	V
I_D	drain current	$T_c = 25\text{ °C}$	[2]	-	-	111	A
		$T_c = 100\text{ °C}$	[2]	-	-	78	A
I_{DM}	peak drain current	pulsed; t_p limited by T_j (max)	[3]	-	-	284	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 18\text{ V}$; $I_D = 71\text{ A}$; $T_j = 25\text{ °C}$	-	17	26	mΩ	

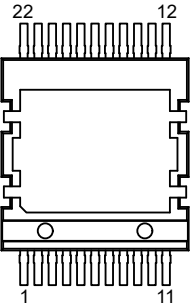
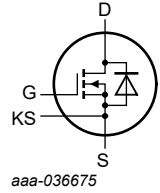
[1] Recommended turn off gate voltage is -5 V to 0 V. Recommended turn on gate voltage is 15 V to 18 V. Do not use with $V_{GSon} < 13\text{ V}$.

[2] Limited by the maximum values of T_j , $R_{th(j-c)}$ and $R_{DSon}(T_j)$.

[3] Designed value (not tested).

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view</p> <p>QDPAK (SOT8114-1)</p>	 <p>aaa-036675</p>
2	KS	Kelvin source		
3 to 11	S	source		
12 to 22	D	drain		
HS	D	heatsink, connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NSF017120T1A0	QDPAK	Plastic, surface-mounted top side cooling (TSC) package; 22 leads; 1.14 mm pitch; 15.0 × 15.4 mm × 2.3 mm body	SOT8114-1

7. Marking

Table 4. Marking codes

Type number	Marking code
NSF017120T1A0	NSF017120T1A0

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	1200	V
V_{GS}	gate-source voltage		[1]	-10	22	V
I_D	drain current	$T_c = 25\text{ °C}$	[2]	-	111	A
		$T_c = 100\text{ °C}$	[2]	-	78	A
I_{DM}	peak drain current	pulsed; t_p limited by T_j (max)	[3]	-	284	A
P_{tot}	total power dissipation	$T_c = 25\text{ °C}$		-	469	W
T_j	junction temperature			-55	175	°C
T_{stg}	storage temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_c = 25\text{ °C}$	[2]	-	86	A
I_{SM}	peak source current	pulsed; limited by T_j (max)	[3]	-	213	A

[1] Recommended turn off gate voltage is -5 V to 0 V. Recommended turn on gate voltage is 15 V to 18 V. Do not use with $V_{GSon} < 13\text{ V}$.

[2] Limited by the maximum values of T_j , $R_{th(j-c)}$ and $R_{DSon}(T_j)$.

[3] Designed value (not tested).

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case			-	0.24	0.32	K/W

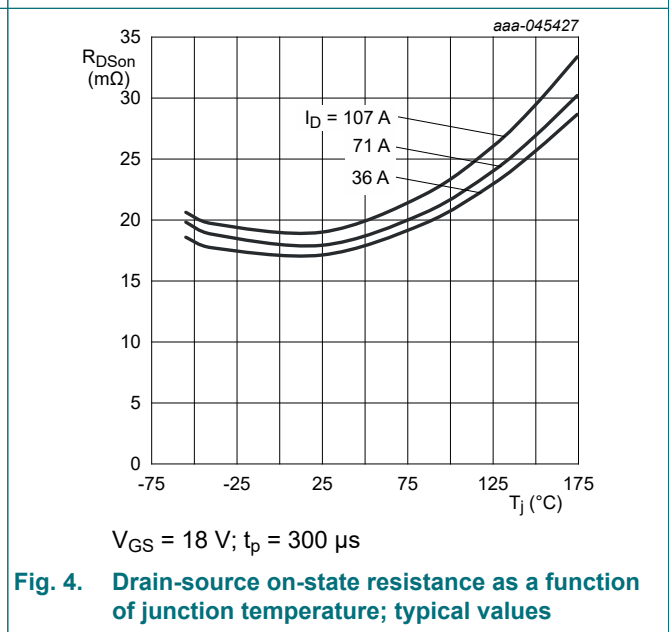
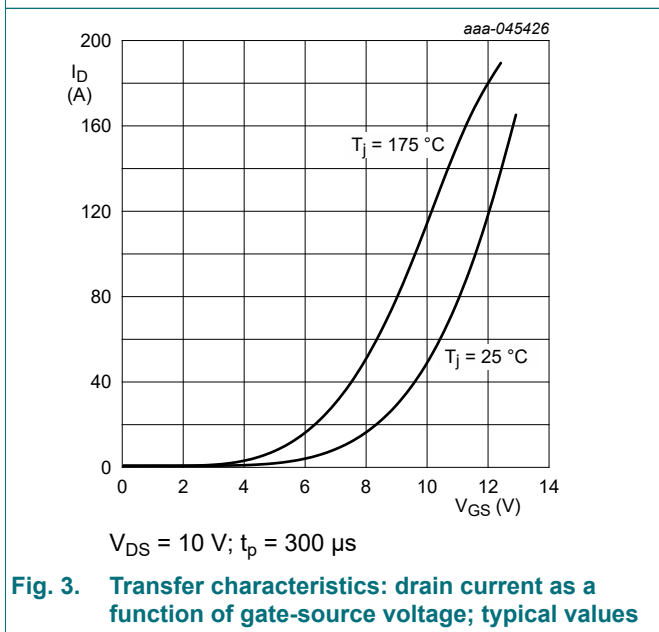
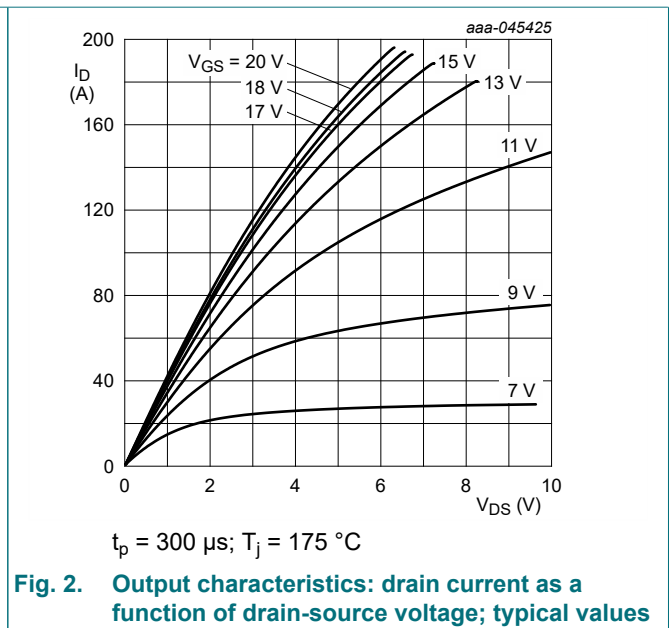
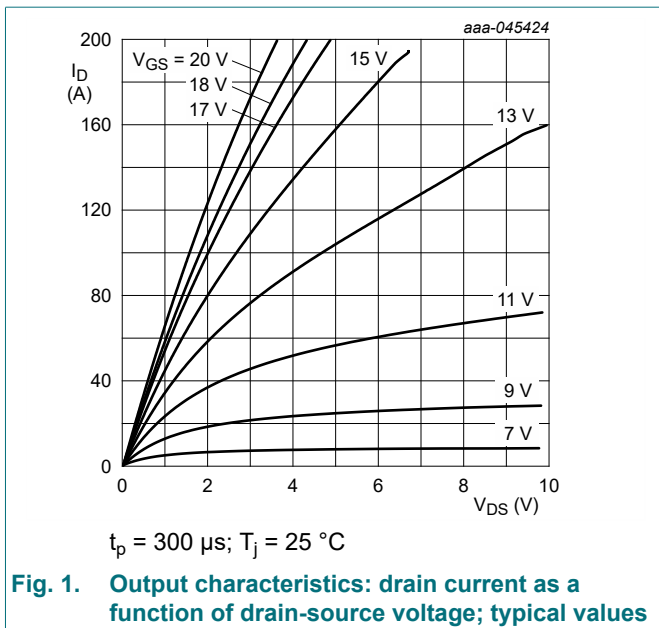
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 1 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	1200	-	-	V	
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 7.1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	[1]	1.7	2.3	2.9	V
		$I_D = 35 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	[1]	-	2.77	-	V
I_{DSS}	drain leakage current	$V_{DS} = 1200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	μA	
I_{GSS}	gate leakage current	$V_{GS} = 22 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 18 \text{ V}; I_D = 71 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	17	26	mΩ	
		$V_{GS} = 18 \text{ V}; I_D = 71 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	30	-	mΩ	
		$V_{GS} = 15 \text{ V}; I_D = 71 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	22	-	mΩ	
		$V_{GS} = 15 \text{ V}; I_D = 71 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	32	-	mΩ	
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 71 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	32	-	S	
$R_{G(int)}$	internal gate resistance	$f = 0.5 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	0.75	-	Ω	
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DD} = 800 \text{ V}; I_D = 71 \text{ A}; V_{GS} = -5/+18 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	196	-	nC	
Q_{GS}	gate-source charge		-	79	-	nC	
Q_{GD}	gate-drain charge		-	49	-	nC	
C_{iss}	input capacitance	$V_{DD} = 800 \text{ V}; f = 500 \text{ kHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	4690	-	pF	
C_{oss}	output capacitance		-	240	-	pF	
C_{rss}	reverse transfer capacitance		-	5	-	pF	
$C_{o(er)}$	effective output capacitance, energy related		$V_{DD} = 800 \text{ V}; V_{GS} = 0 \text{ V}; f = 500 \text{ kHz};$ Calculated based on C_{oss} ; $T_j = 25 \text{ }^\circ\text{C}$	-	300	-	pF
$C_{o(tr)}$	effective output capacitance, time related		-	429	-	pF	
Q_{oss}	output capacitance charge		-	343	-	nC	
E_{oss}	C_{oss} stored energy		-	96	-	μJ	
$t_{d(on)}$	turn-on delay time	$V_{DD} = 800 \text{ V}; I_D = 71 \text{ A}; R_{G(ext)} = 4.7 \text{ }^\circ\Omega;$ $L_L = 34.9 \text{ }^\circ\mu\text{H}; V_{GS} = -5/+18 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	40	-	ns	
t_r	rise time		-	16	-	ns	
$t_{d(off)}$	turn-off delay time		-	42	-	ns	
t_f	fall time		-	11	-	ns	
E_{on}	turn-on switching loss		-	1369	-	μJ	
E_{off}	turn-off switching loss		-	209	-	μJ	
Source-drain diode							
V_{SD}	source-drain voltage	$V_{DD} = 800 \text{ V}; I_S = 71 \text{ A}; V_{GS} = -5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	4.4	-	V	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$V_{DD} = 800\text{ V}; I_S = 71\text{ A}; V_{GS} = -5\text{ V};$ $di_S/dt = -7038\text{ A}/\mu\text{s}; T_j = 175\text{ }^\circ\text{C}$	-	28	-	ns
		$V_{DD} = 800\text{ V}; I_S = 71\text{ A}; V_{GS} = -5\text{ V};$ $di_S/dt = -2445\text{ A}/\mu\text{s}; T_j = 175\text{ }^\circ\text{C}$	-	49	-	ns
Q_r	recovered charge	$V_{DD} = 800\text{ V}; I_S = 71\text{ A}; V_{GS} = -5\text{ V};$ $di_S/dt = -7038\text{ A}/\mu\text{s}; T_j = 175\text{ }^\circ\text{C}$	-	1584	-	nC
		$V_{DD} = 800\text{ V}; I_S = 71\text{ A}; V_{GS} = -5\text{ V};$ $di_S/dt = -2445\text{ A}/\mu\text{s}; T_j = 175\text{ }^\circ\text{C}$	-	1404	-	nC
I_{RRM}	peak reverse recovery current	$V_{DD} = 800\text{ V}; I_S = 71\text{ A}; V_{GS} = -5\text{ V};$ $di_S/dt = -7038\text{ A}/\mu\text{s}; T_j = 175\text{ }^\circ\text{C}$	-	78	-	A
		$V_{DD} = 800\text{ V}; I_S = 71\text{ A}; V_{GS} = -5\text{ V};$ $di_S/dt = -2445\text{ A}/\mu\text{s}; T_j = 175\text{ }^\circ\text{C}$	-	39	-	A

[1] Measured according to JEP183.



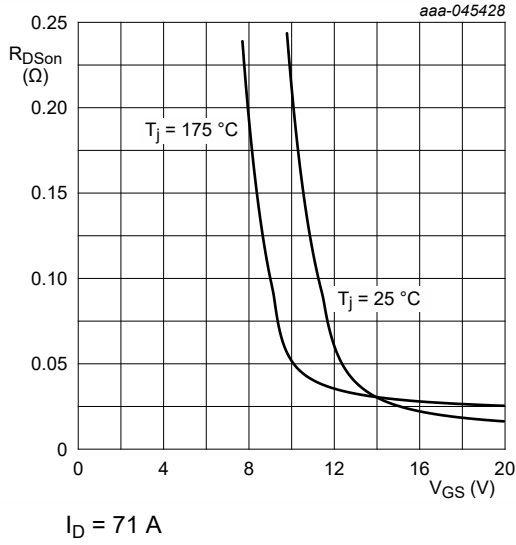


Fig. 5. Drain-source on-state resistance as a function of gate-source voltage

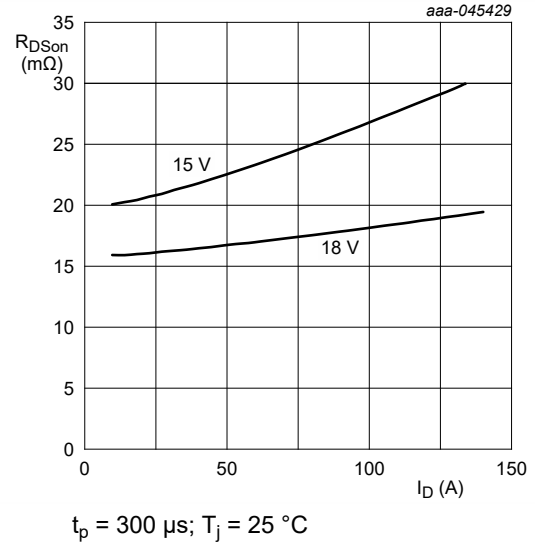


Fig. 6. Drain-source on-state resistance as a function of drain current; typical values

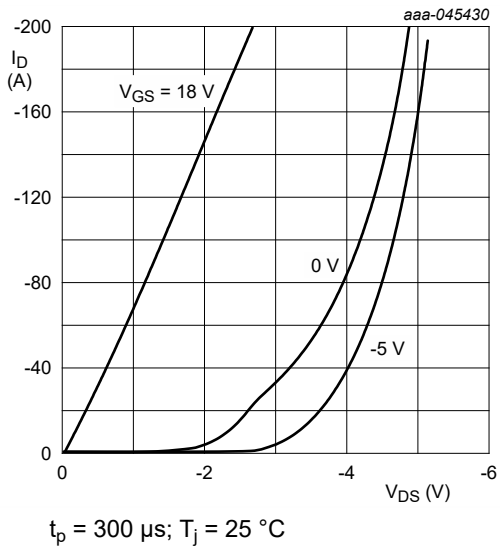


Fig. 7. Drain current as a function of drain-source voltage; typical values (third quadrant characteristics)

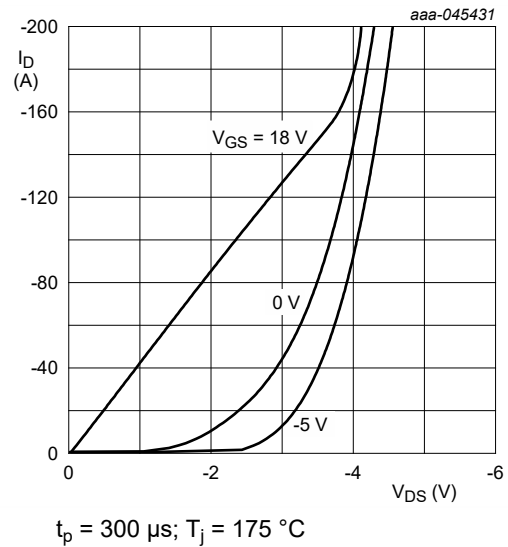


Fig. 8. Drain current as a function of drain-source voltage; typical values (third quadrant characteristics)

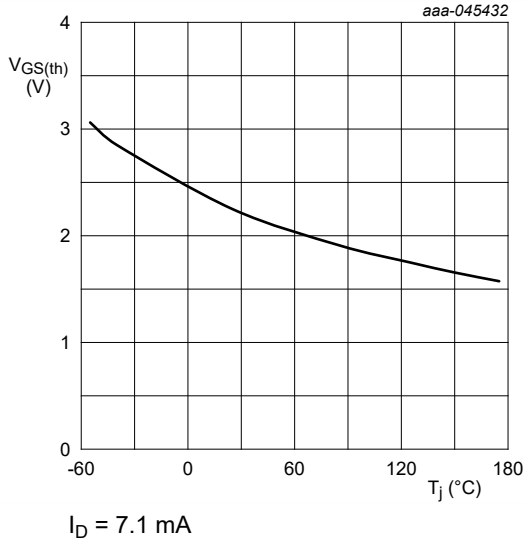


Fig. 9. Gate-source threshold voltage as a function of junction temperature; typical values

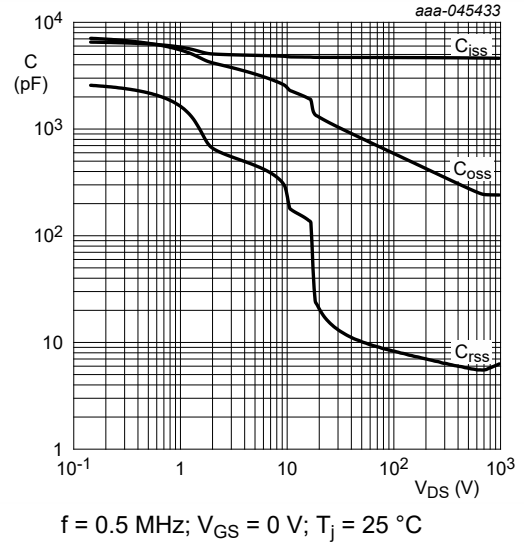


Fig. 10. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

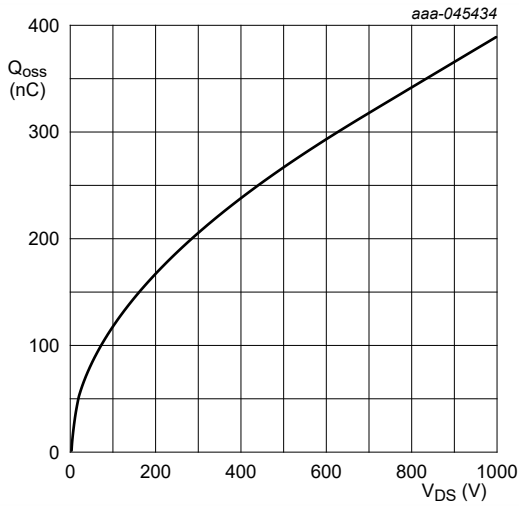


Fig. 11. Output capacitance charge as a function of drain-source voltage; typical values

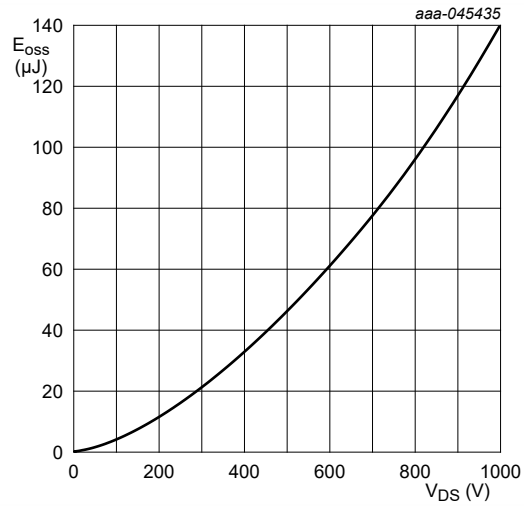
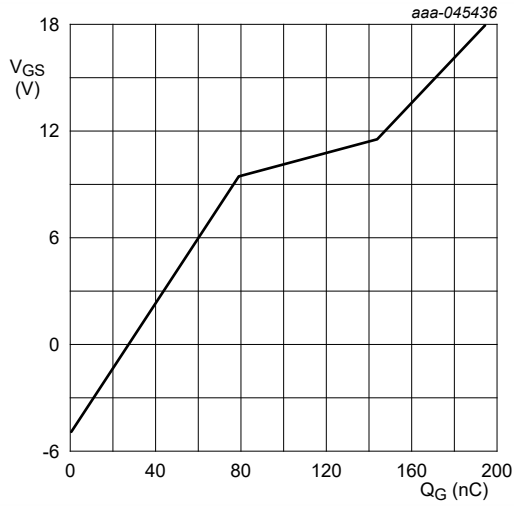
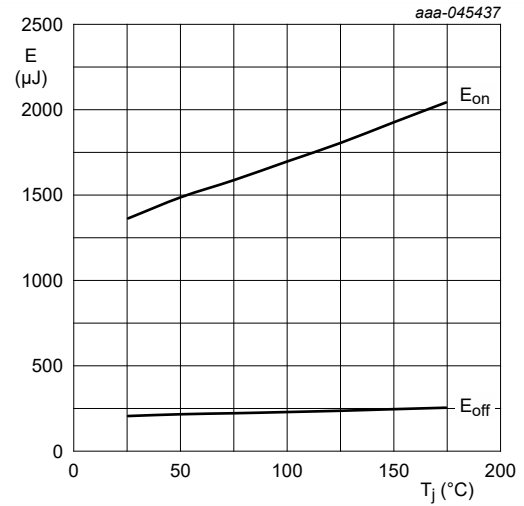


Fig. 12. C_{oss} stored energy as a function of drain-source voltage; typical values



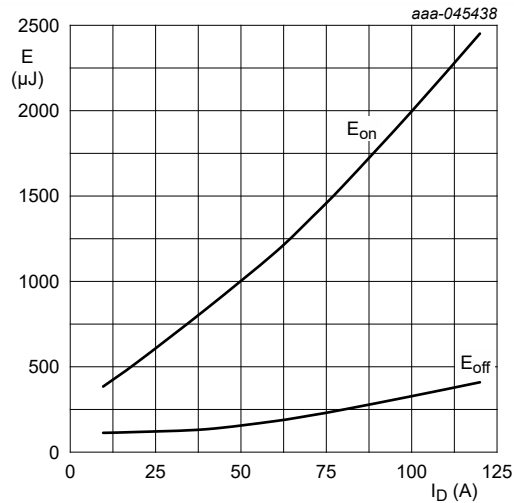
$V_{DD} = 800 \text{ V}; I_D = 71 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values



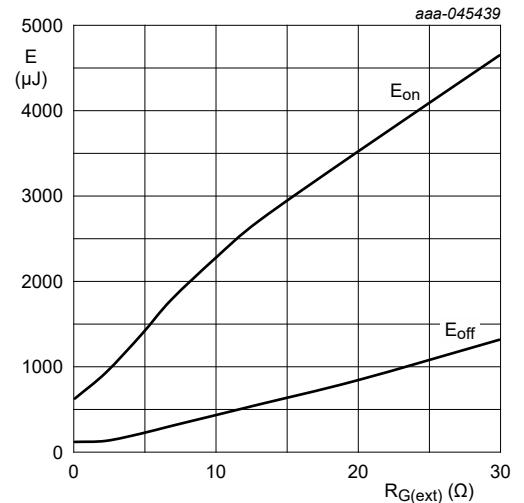
$V_{DD} = 800 \text{ V}; I_D = 71 \text{ A}; V_{GS} = -5/18 \text{ V}; R_{G(\text{ext})} = 4.7 \text{ } \Omega; L_L = 34.9 \text{ } \mu\text{H}$

Fig. 14. Switching loss as a function of junction temperature; typical values



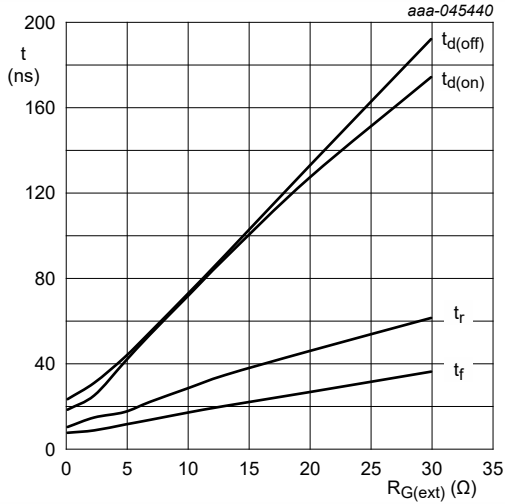
$V_{DD} = 800 \text{ V}; V_{GS} = -5/18 \text{ V}; R_{G(\text{ext})} = 4.7 \text{ } \Omega; L_L = 34.9 \text{ } \mu\text{H}; T_j = 25 \text{ }^\circ\text{C}$

Fig. 15. Switching loss as a function of drain current; typical values



$V_{DD} = 800 \text{ V}; I_D = 71 \text{ A}; V_{GS} = -5/18 \text{ V}; L_L = 34.9 \text{ } \mu\text{H}; T_j = 25 \text{ }^\circ\text{C}$

Fig. 16. Switching loss as a function of external gate resistance; typical values



$V_{DD} = 800 \text{ V}$; $I_D = 71 \text{ A}$; $V_{GS} = -5/18 \text{ V}$; $L_L = 34.9 \mu\text{H}$; $T_j = 25 \text{ }^\circ\text{C}$

Fig. 17. Switching times as a function of external gate resistance; typical values

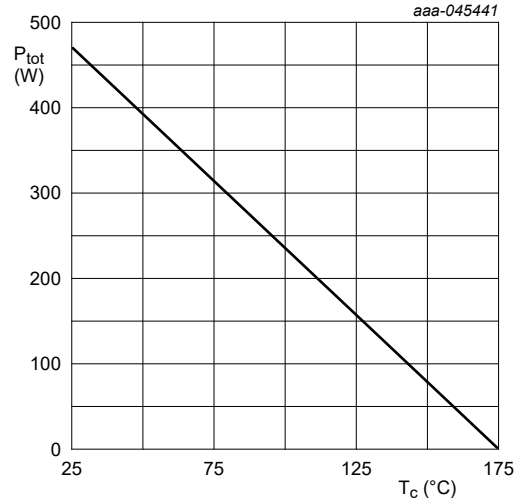


Fig. 18. Power dissipation derating as a function of case temperature; maximum values

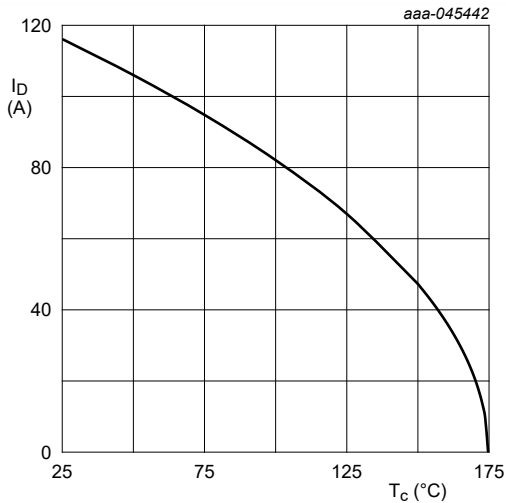
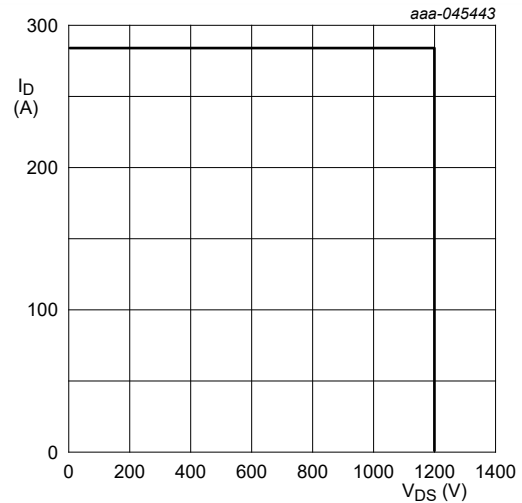


Fig. 19. Continuous drain current as a function of case temperature; maximum values



$V_{GS} = -5/+18 \text{ V}$; $T_c = 25 \text{ }^\circ\text{C}$; $T_j \leq 175 \text{ }^\circ\text{C}$; not for linear use

Fig. 20. Reverse bias safe operating area (RBSOA)

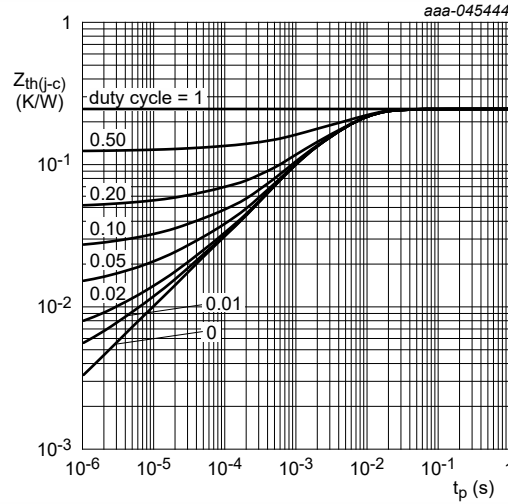


Fig. 21. Transient thermal impedance from junction to case as a function of pulse duration; typical values

11. Test information

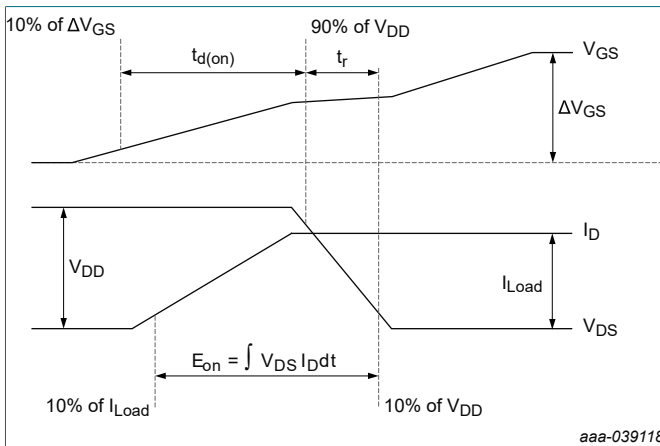


Fig. 22. Definition of switching times and losses during channel turn-on

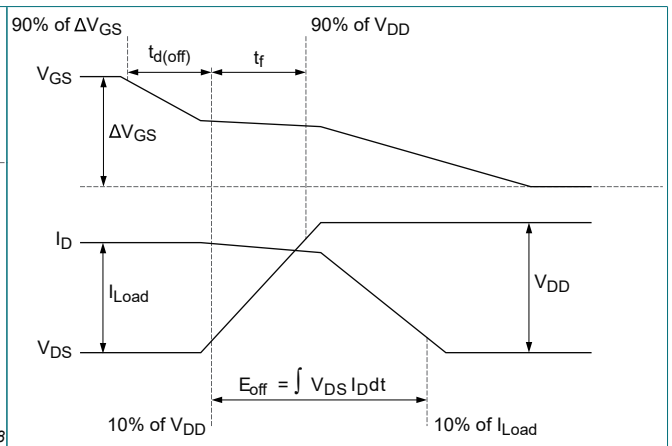


Fig. 23. Definition of switching times and losses during channel turn-off

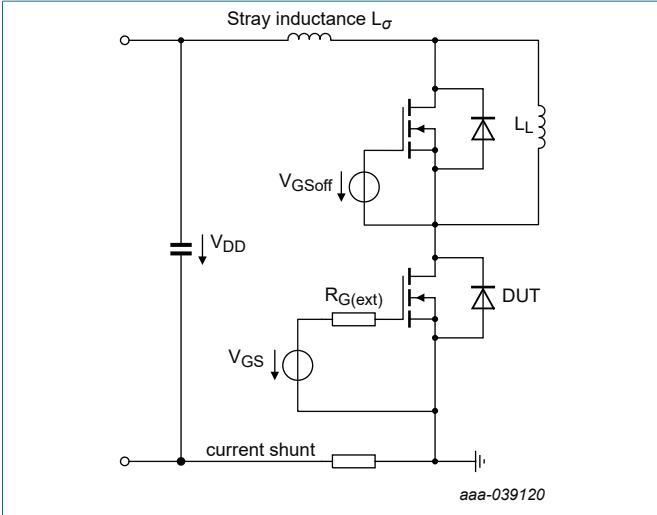


Fig. 24. Test circuit for dynamic characterization of channel and gate charge characteristics

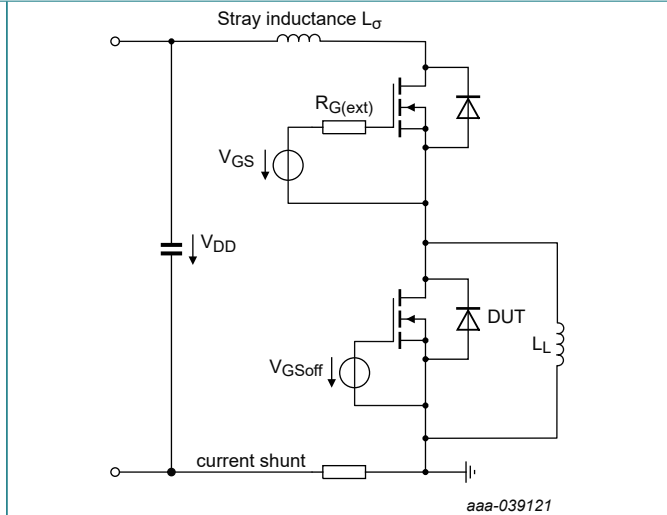


Fig. 25. Test circuit for dynamic characterization of body diode

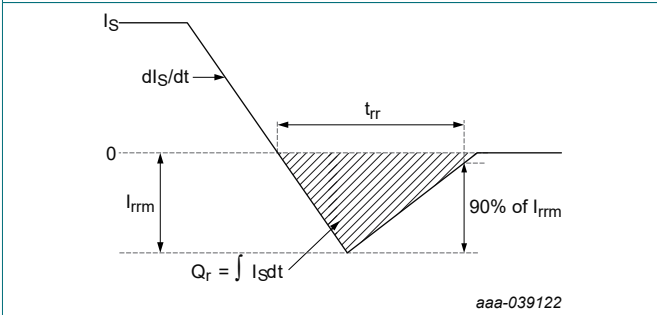


Fig. 26. Definition of dynamic characteristics of body diode

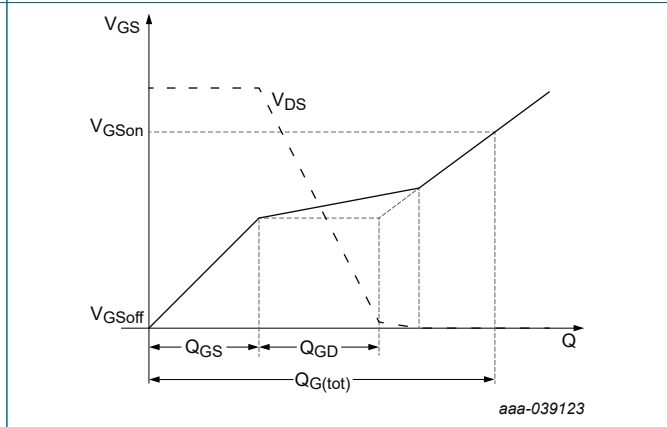


Fig. 27. Definition of gate charge characteristics

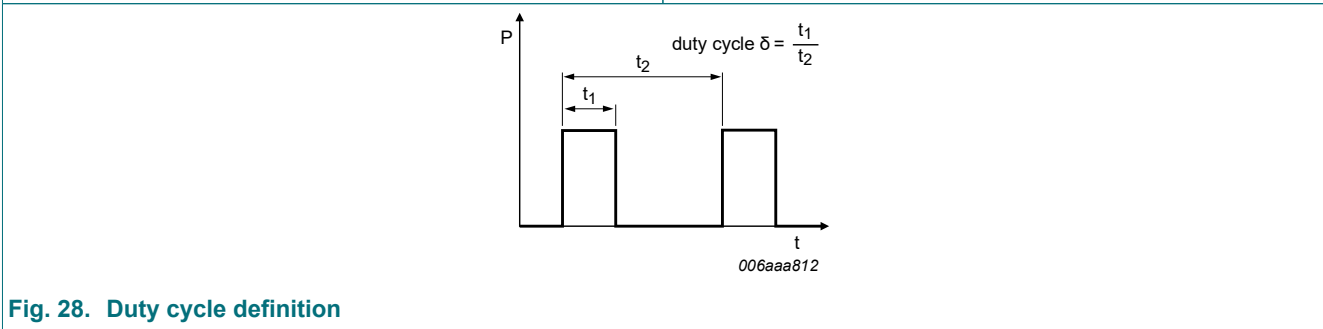


Fig. 28. Duty cycle definition

12. Package outline

Plastic, surface-mounted top side cooling (TSC) package; 22 leads; 1.14 mm pitch; 15.0 × 15.4 mm × 2.3 mm body

SOT8114-1

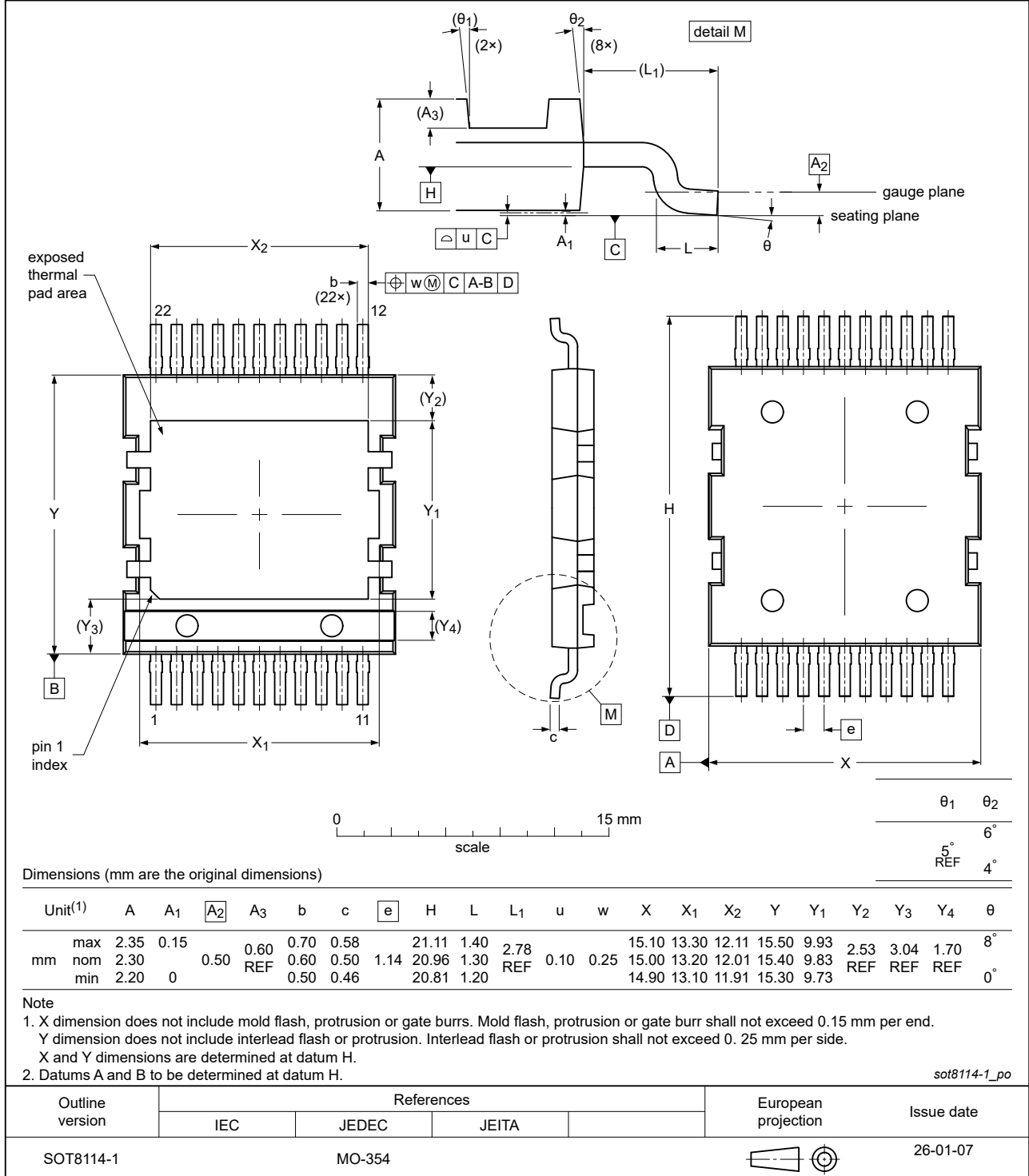


Fig. 29. Package outline QDPAK (SOT8114-1)

13. Soldering

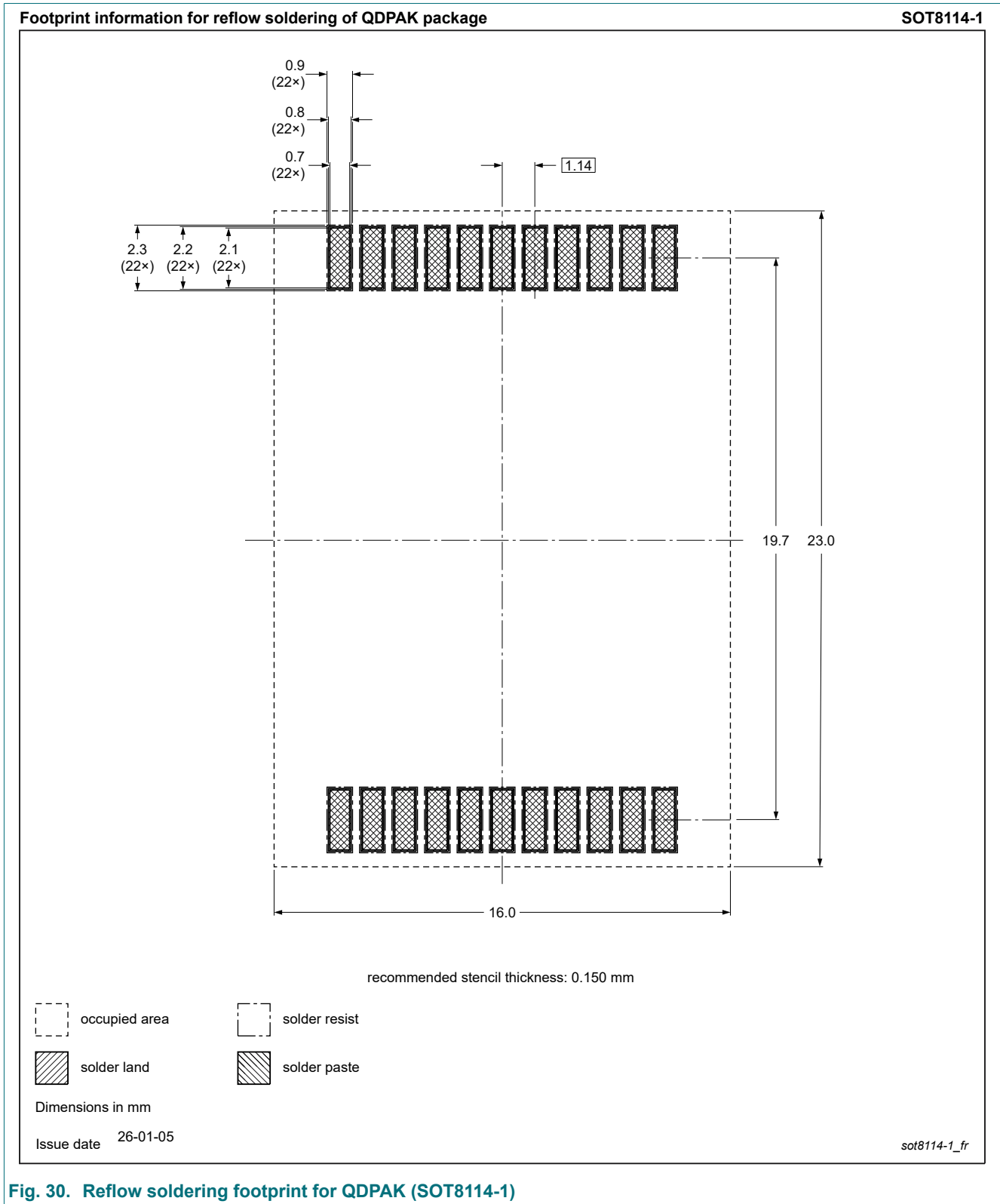


Fig. 30. Reflow soldering footprint for QDPAK (SOT8114-1)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NSF017120T1A0 v.1	20260408	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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