LMG2100R044 100-V, 35-A GaN Half-Bridge Power Stage

1 Features

- Integrated 4.4-mΩ GaN FETs and driver
- 80-V continuous, 100-V pulsed voltage rating
- Package optimized for easy PCB layout
- 5-V external bias power supply
- Supports 3.3-V, 5-V and 12-V input logic levels
- High slew rate switching with low ringing
- Gate driver capable of up to 10-MHz switching
- Internal bootstrap supply voltage clamping to prevent GaN FET Overdrive
- Supply rail undervoltage 4lockout protection
- Excellent propagation delay (29.5-ns typical) and matching (2-ns typical)
- Low power consumption
- Exposed top QFN package for top-side cooling
- Large GND pad for bottom-side cooling

2 Applications

- Buck, boost, buck-boost converters
- LLC converters
- Solar inverters
- Telecom and server power
- Motor drives
- Power tools
- Class-D audio amplifiers

3 Description

The LMG2100R044 device is an 80-V continuous, 100-V pulsed, 35-A half-bridge power stage, with integrated gate-driver and enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two 100-V GaN FETs driven by one high-frequency 80-V GaN FET driver in a half-bridge configuration.

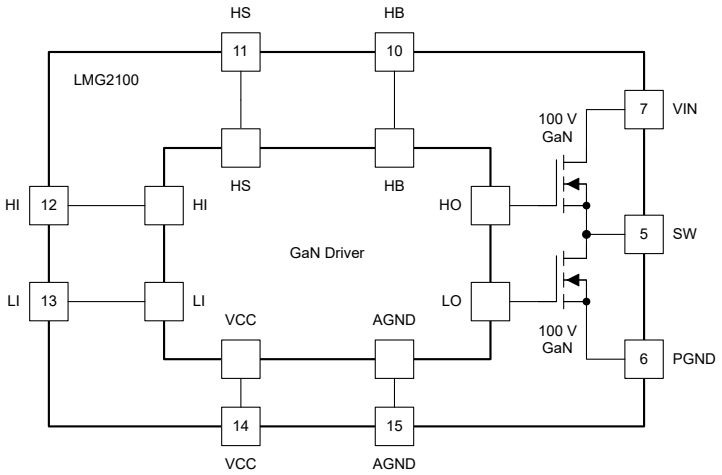
GaN FETs provide significant advantages for power conversion as they have near zero reverse recovery and very small input capacitance C_{ISS} and output capacitance C_{OSS}. All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements. The LMG2100R044 device is available in a 5.5 mm × 4.5 mm × 0.89 mm lead-free package and can be easily mounted on PCBs.

The TTL logic compatible inputs can withstand input voltages up to 12 V regardless of the VCC voltage. The proprietary bootstrap voltage clamping technique ensures the gate voltages of the enhancement mode GaN FETs are within a safe operating range.

The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. It is an ideal solution for applications requiring high-frequency, high-efficiency operation in a small form factor.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMG2100R044	VQFN (16)	5.50 mm × 4.50 mm



Simplified Block Diagram

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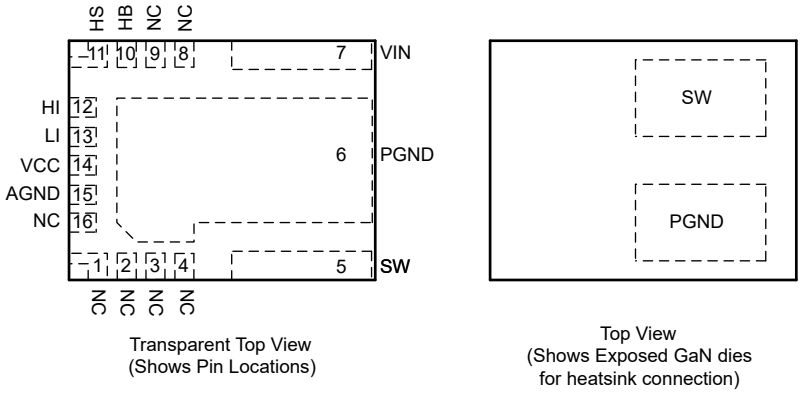
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2023	*	Advance Information release

5 Pin Configuration and Functions



Transparent Top View
(Shows Pin Locations)

Top View
(Shows Exposed GaN dies
for heatsink connection)

Figure 5-1. RAR Package 16-Pin VQFN Top View

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
NC	1-4, 8, 9, 16	-	Not connected internally. Leave floating.
SW	5	P	Switching node. Electrically shorted to HS pin. Ensure low capacitance at this node on PCB.
PGND	6	G	Power ground. Low-side GaN FET source. Electrically shorted to AGND pin.
VIN	7	P	Input voltage pin. Electrically connected to high-side GaN FET drain.
HB	10	P	High-side gate driver bootstrap rail.
HS	11	P	High-side GaN FET source connection
HI	12	I	High-side gate driver control input
LI	13	I	Low-side driver control input
VCC	14	P	5-V positive gate drive supply
AGND	15	G	Analog ground. Ground of driver device.

(1) I = Input, O = Output, G = Ground, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	MIN	MAX	UNIT
VIN to PGND	0	80	V
VIN to PGND (pulsed, 100-ms max duration)(2)		100	V
HB to AGND	-0.3	86	V
HS to AGND	-5	80	V
HI to AGND	-0.3	12	V
LI to AGND	-0.3	12	V
VCC to AGND	-0.3	6	V
HB to HS	-0.3	6	V
HB to VCC	0	80	V
SW to PGND	-5	80	V
IOUT from SW pin (Continuous), T_J = 25℃		35	A
IOUT from SW pin (Pulsed, 300 µs), T_J = 25℃		125	A
Junction Temperature, T_J	-40	150	°C
Storage Temperature, T_{stg}	-40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device can withstand 1000 pulses up to 100V of 100ms duration and less than 1% duty cycle over its lifetime.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC		4.75	5	5.25	V
LI or HI Input		0		12	V
VIN		0		80	V
HS, SW		-5		80	V
HB		V_{HS}+ 4		V_{HS}+ 5.25	V
t_{PW}	Minimum input pulse width supported	10			ns
HS, SW Slew rate(1)				50	V/ns
Junction Temperature, T_J		-40		125	°C

(1) This parameter is guaranteed by design. Not tested in production.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

THERMAL METRIC (1)		LMG2100R044 QFN 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1	
$R_{\theta JB}$	Junction-to-board thermal resistance	2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953 .

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{CC}	VCC Quiescent Current	LI = HI = 0V, VCC = 5V, HB-HS = 4.6V		0.09	0.125	mA
I_{CC}	VCC Quiescent Current	LI=VCC=5V, HI=0V, HB-HS=4.6V		0.460	7	mA
I_{CCO}	Total VCC Operating Current	f = 500 kHz, 50% Duty cycle, V_{IN} = 48V		7.0	10	mA
I_{HB}	HB Quiescent Current	LI = HI = 0V, VCC = 5V, HB-HS = 4.6V		0.1	0.150	mA
I_{HBO}	HB Operating Current	f = 500 kHz, 50% Duty cycle, V_{DD} = 5V, V_{IN} = 0V		3.3	5	mA
INPUT PINS						
V_{IH}	High-Level Input Voltage Threshold	Rising Edge	1.87	2.06	2.22	V
V_{IL}	Low-Level Input Voltage Threshold	Falling Edge	1.48	1.66	1.76	V
V_{HYS}	Hysteresis between rising and falling threshold			400		mV
R_I	Input pull down resistance		100	200	300	kΩ
UNDER VOLTAGE PROTECTION						
V_{CCR}	VCC Rising edge threshold	Rising	3.2	3.8	4.5	V
V_{CCF}	VCC Falling edge threshold		3.0	3.6	4.3	V
$V_{CC(hyst)}$	VCC UVLO threshold hysteresis			200		mV
V_{HBR}	HB Rising edge threshold	Rising	2.5	3.2	3.9	V
V_{HBF}	HB Falling edge threshold		2.3	3.0	3.7	V
$V_{HB(hyst)}$	HB UVLO threshold hysteresis			200		mV
BOOTSTRAP DIODE						
V_{DL}	Low-Current forward voltage	I_{VDD-HB} = 100µA		0.45	0.65	V
V_{DH}	High current forward voltage	I_{VDD-HB} = 100mA		0.9	1.0	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100mA		1.85	2.8	Ω
	HB-HS Clamp	Regulation Voltage	4.65	5	5.2	V
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, IR = 100 mA		40		ns
Q_{RR}	Bootstrap diode reverse recovery charge	V_{VIN} = 50 V		2		nC
POWER STAGE						
$R_{DS(ON)HS}$	High-side GaN FET on-resistance	LI=0V, HI=VCC=5V, HB-HS=5V, I(VIN-SW)=16A, T_J = 25°C		4.4	5.7	mΩ
$R_{DS(ON)LS}$	Low-side GaN FET on-resistance	LI=VCC=5V, HI=0V, HB-HS=5V, I(SW-PGND)=16A, T_J = 25°C		4.4	5.4	mΩ
V_{SD}	GaN 3rd quadrant conduction drop	I_{SD} = 500 mA, V_{IN} floating, VCC = 5 V, HI = LI = 0V		1.6		V
$I_{L-VIN-SW}$	Leakage from VIN to SW when the high-side GaN FET and low-side GaN FET are off	VIN = 80V, SW=0, HI = LI = 0V, VCC = 5V, T_J=25°C		40	200	µA
$I_{L-SW-GND}$	Leakage from SW to GND when the high-side GaN FET and low-side GaN FET are off	SW = 80V, HI = LI = 0V, VCC = 5V, T_J=25°C		40	200	µA

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over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OSS}	Output Capacitance of high-side GaN FET or low-side GaN FET	V_{DS}=50V, V_{GS}= 0V (HI = LI = 0V)		304	456	pF
$C_{OSS(ER)}$	Output Capacitance of high-side GaN FET or low-side GaN FET - Energy Related	V_{DS}=0 to 50V, V_{GS}= 0V (HI = LI = 0V)		401		pF
$C_{OSS(TR)}$	Output Capacitance of high-side GaN FET or low-side GaN FET - Time Related	V_{DS}=0 to 50V, V_{GS}= 0V (HI = LI = 0V)		501		pF
C_{WELL}	HV-Well Capacitance (SW to PGND)	V_{IN}=V_{SW}=50V, HI = LI = 0V		30		pF
Q_G	Total Gate Charge of high side or low side HEMT	V_{DS}=50V, I_D= 16A, V_{GS}= 5V		7.2		nC
Q_{GD}	Gate to Drain Charge of high side or low side HEMT	V_{DS}=50V, I_D= 16A		0.8		nC
Q_{GS}	Gate to Source Charge of high side or low side HEMT	V_{DS}=50V, I_D= 16A		1.8		nC
Q_{OSS}	Output Charge (sum of high side HEMT, low side HEMT and gate-driver HV-Well charge)	V_{DS}=50V, I_D= 16A		55	84	nC
Q_{RR}	Source to Drain Reverse Recovery Charge	Not including internal driver bootstrap diode		0		nC
t_{HIPLH}	Propagation delay: HI Rising(2)	LI=0V, VCC=5V, HB-HS=5V, VIN=48V		29.5	50	ns
t_{HIPHL}	Propagation delay: HI Falling(2)	LI=0V, VCC=5V, HB-HS=5V, VIN=48V		29.5	50	ns
t_{LPLH}	Propagation delay: LI Rising(2)	HI=0V, VCC=5V, HB-HS=5V, VIN=48V		29.5	50	ns
t_{LPHL}	Propagation delay: LI Falling(2)	HI=0V, VCC=5V, HB-HS=5V, VIN=48V		29.5	50	ns
t_{MON}	Delay Matching: LI high & HI low(2)			2	8.0	ns
t_{MOFF}	Delay Matching: LI low & HI high(2)			2	8.0	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			10		ns

(1) Parameters that show only a typical value are guaranteed by design and may not be tested in production
(2) See *Propagation Delay and Mismatch Measurement* section

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7 Typical Characteristics

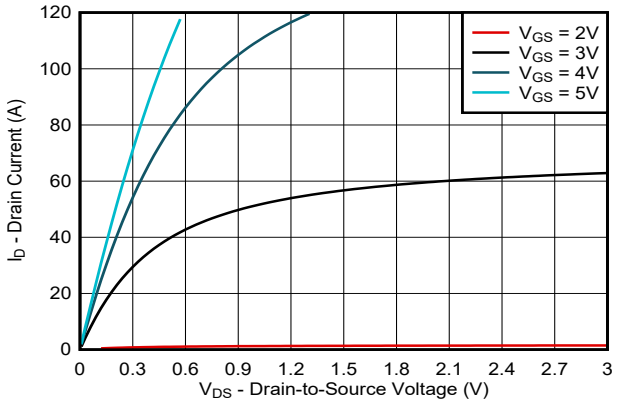
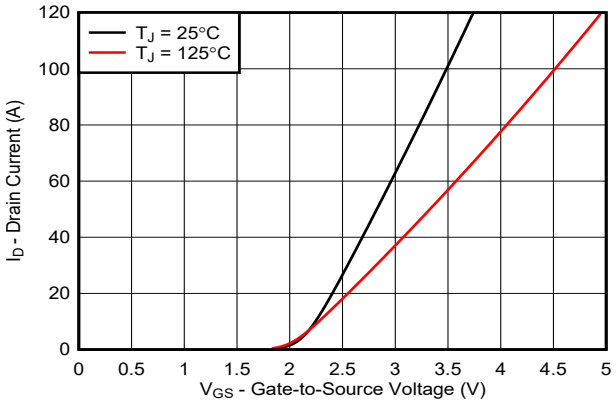


Figure 7-1. Typical Output Characteristics at 25°C



V_{DS} = 3 V

Figure 7-2. Typical Transfer Characteristics

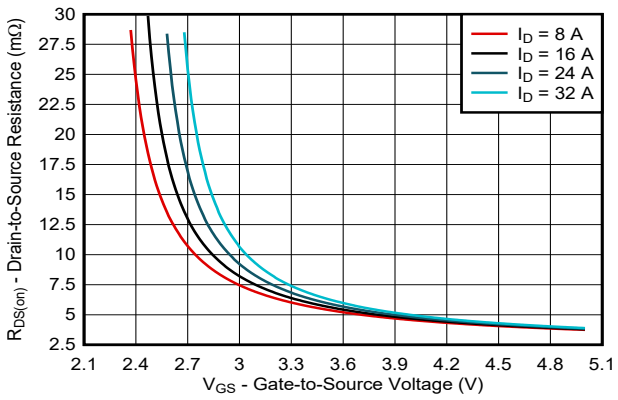
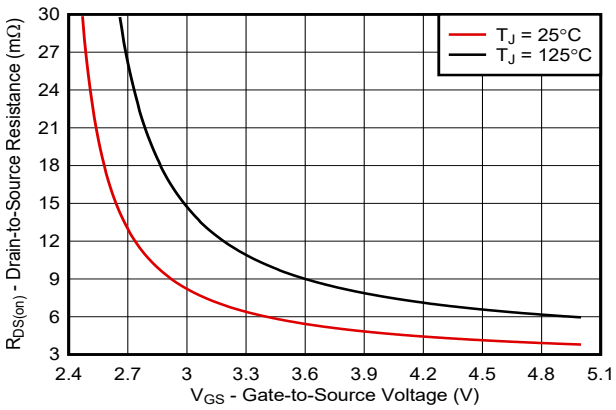


Figure 7-3. $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents



I_D = 16 A

Figure 7-4. Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

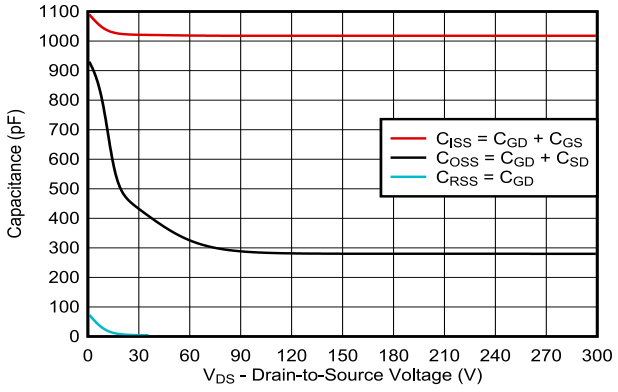


Figure 7-5. Typical Capacitance (Linear Scale)

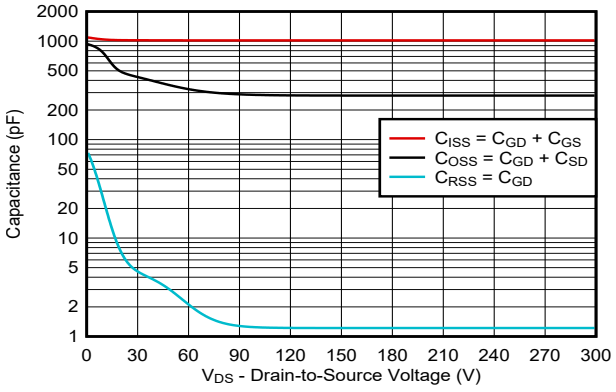


Figure 7-6. Typical Capacitance (Log Scale)

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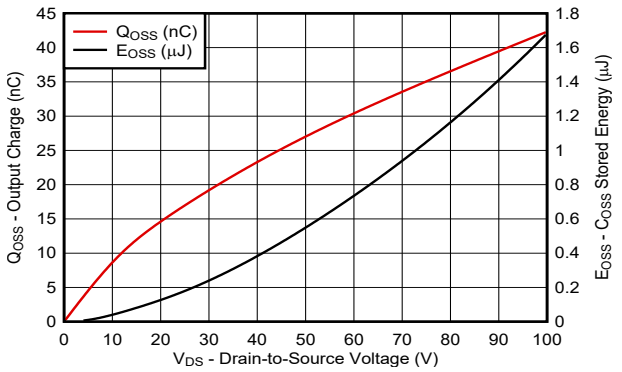
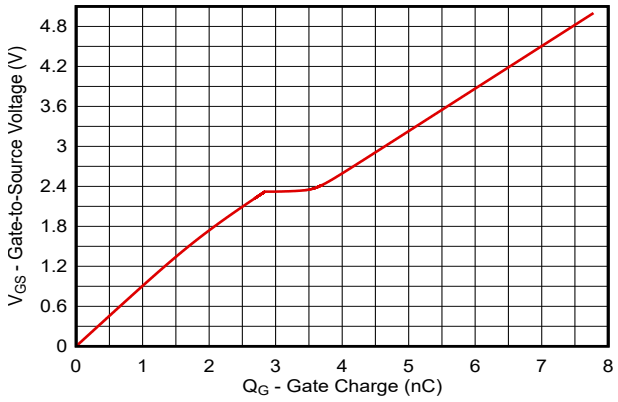
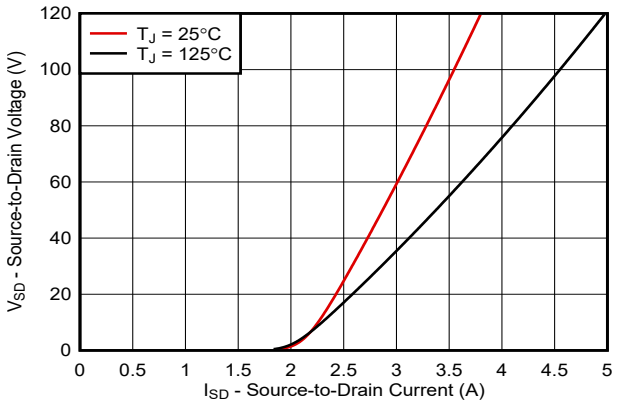


Figure 7-7. Typical Output Charge and C_{OSS} Stored Energy



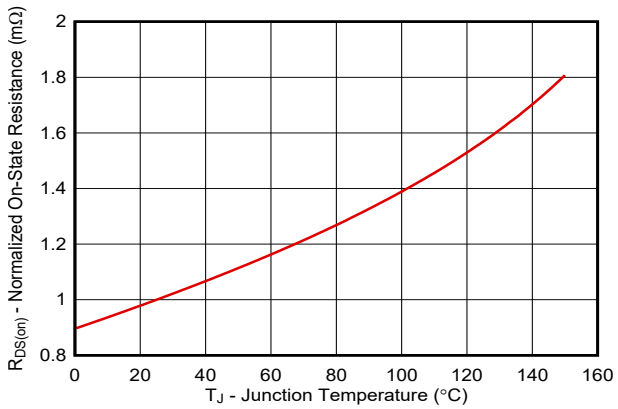
I_D = 16 A V_{DS} = 50 V

Figure 7-8. Typical Gate Charge



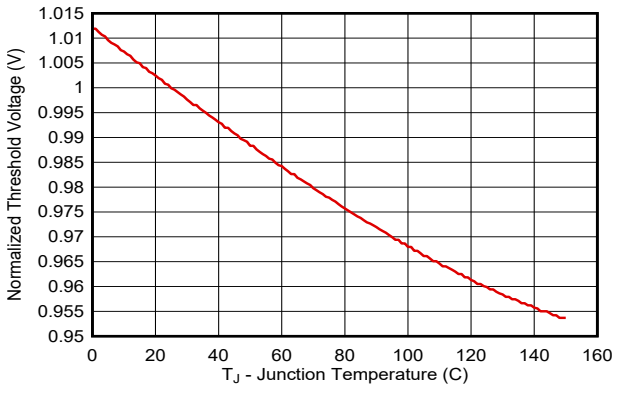
V_{GS} = 0 V

Figure 7-9. Reverse Drain-Source Characteristics



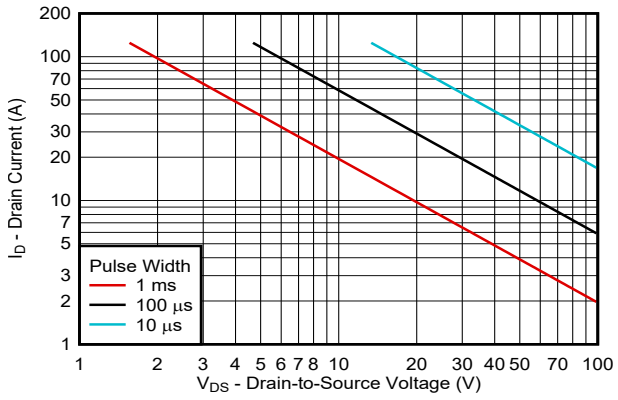
I_D = 16 A V_{GS} = 5 V

Figure 7-10. Normalized On-State Resistance vs.Temperature



I_D = 4.2 mA

Figure 7-11. Normalized Threshold Voltage vs. Temperature



T_J = Max Rated T_C = 25 °C Single Pulse

Figure 7-12. Safe Operating Area

8 Parameter Measurement Information

8.1 Propagation Delay and Mismatch Measurement

Figure 8-1 shows the typical test setup used to measure the propagation mismatch. As the gate drives are not accessible, pullup and pulldown resistors in this test circuit are used to indicate when the low-side GaN FET turns ON and the high-side GaN FET turns OFF and vice versa to measure the t_{MON} and t_{MOFF} parameters. Resistance values used in this circuit for the pullup and pulldown resistors are in the order of 1 kΩ; the current sources used are 2 A.

Figure 8-2 through Figure 8-5 show propagation delay measurement waveforms. For turnon propagation delay measurements, the current sources are not used. For turnoff time measurements, the current sources are set to 2 A, and a voltage clamp limit is also set, referred to as $VIN_{(CLAMP)}$. When measuring the high-side component turnoff delay, the current source across the high-side FET is turned on, the current source across the low-side FET is off, HI transitions from high-to-low, and output voltage transitions from V_{IN} to $V_{IN(CLAMP)}$. Similarly, for low-side component turnoff propagation delay measurements, the high-side component current source is turned off, and the low-side component current source is turned on, LI transitions from high to low and the output transitions from GND potential to $V_{IN(CLAMP)}$. The time between the transition of LI and the output change is the propagation delay time.

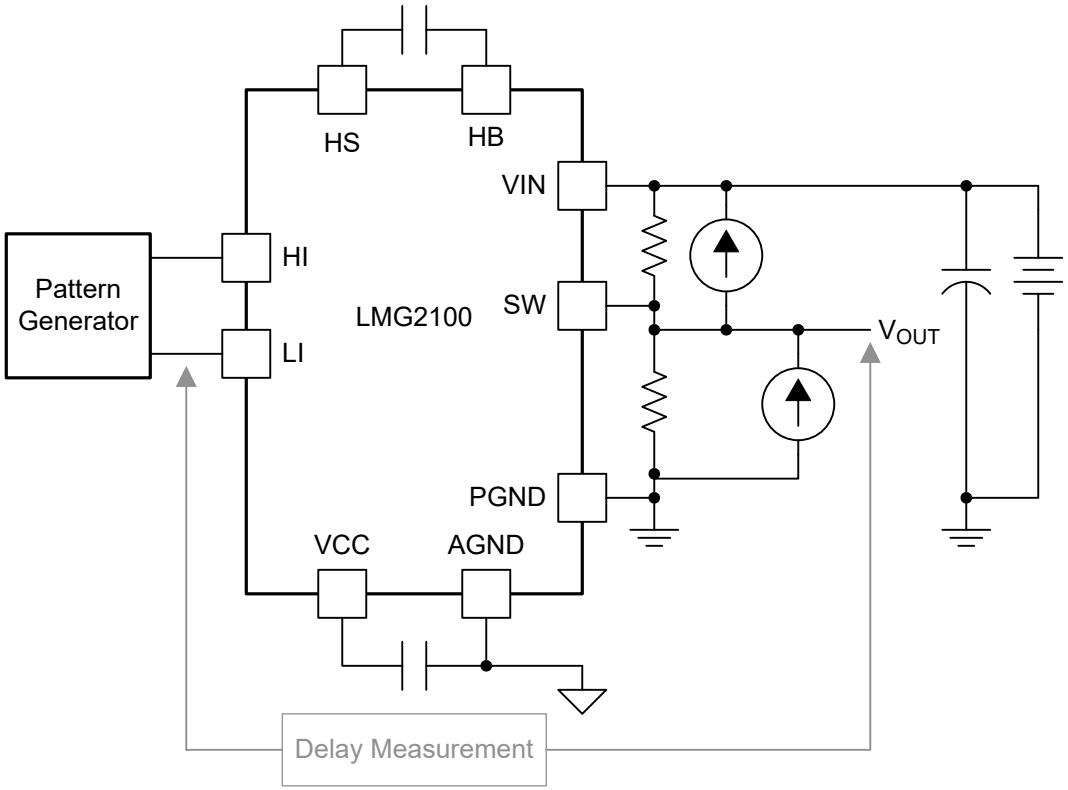


Figure 8-1. Propagation Delay and Propagation Mismatch Measurement

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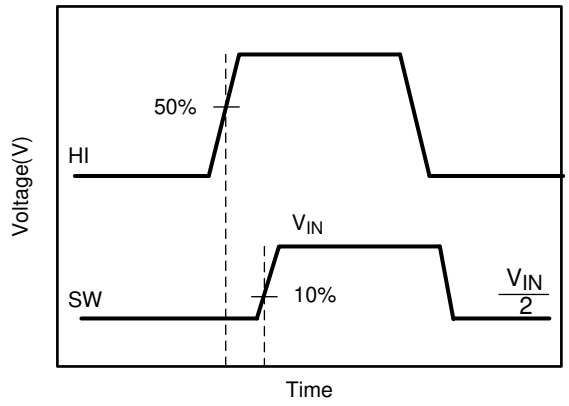

Figure 8-2. High-Side Gate Driver Turnon

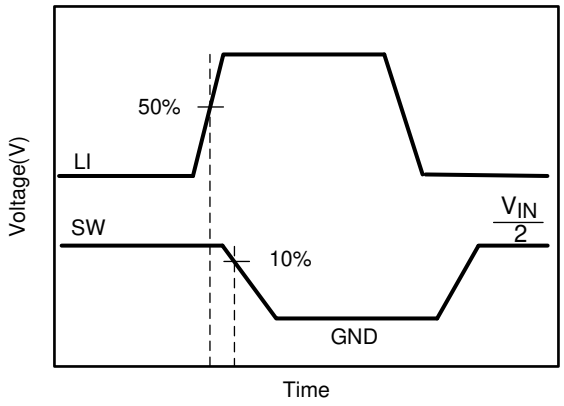

Figure 8-3. Low-Side Gate Driver Turnon

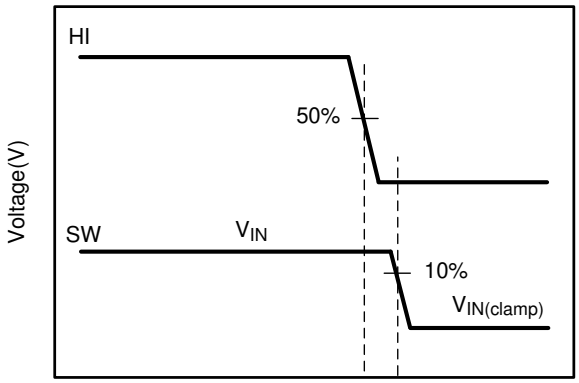

Figure 8-4. High-Side Gate Driver Turnoff

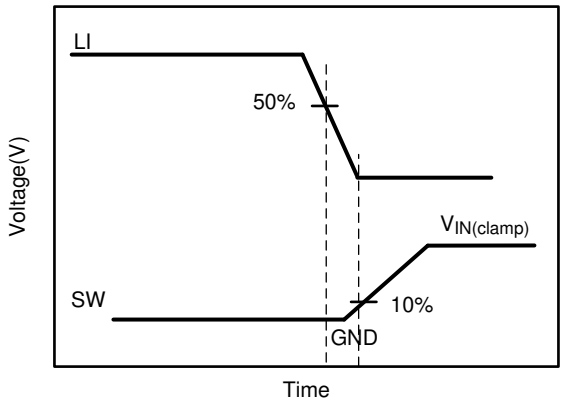

Figure 8-5. Low-Side Gate Driver Turnoff

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9 Detailed Description

9.1 Overview

Figure 9-1 shows the LMG2100R044, half-bridge, GaN power stage with highly integrated high-side and low-side gate drivers, which includes built-in UVLO protection circuitry and an overvoltage clamp circuitry. The clamp circuitry limits the bootstrap refresh operation to ensure that the high-side gate driver overdrive does not exceed 5.4 V. The device integrates two, 4.4-mΩ GaN FETs in a half-bridge configuration. The device can be used in many isolated and non-isolated topologies allowing very simple integration. The package is designed to minimize the loop inductance while keeping the PCB design simple. The drive strengths for turnon and turnoff are optimized to ensure high voltage slew rates without causing any excessive ringing on the gate or power loop.

9.2 Functional Block Diagram

Figure 9-1 shows the functional block diagram of the LMG2100R044 device with integrated high-side and low-side GaN FETs.

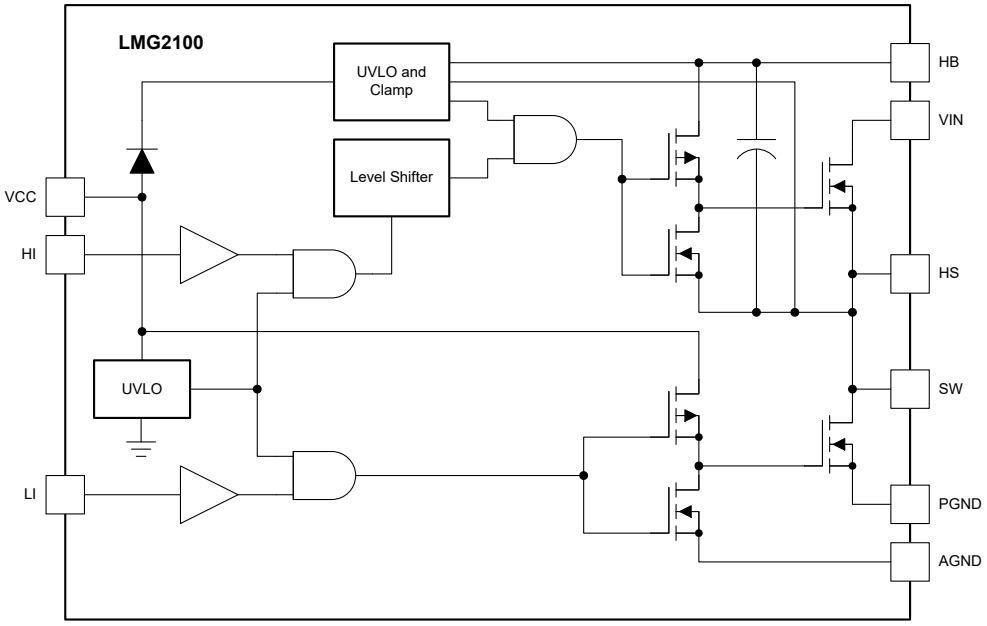

Figure 9-1. Functional Block Diagram

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9.3 Feature Description

The LMG2100R044 device brings ease of designing high power density boards without the need for underfill while maintaining creepage and clearance requirements. The propagation delays between the high-side gate driver and low-side gate driver are matched to allow very tight control of dead time. Controlling the dead time is critical in GaN-based applications to maintain high efficiency. HI and LI can be independently controlled to minimize the third quadrant conduction of the low-side FET for hard switched buck converters. A very small propagation mismatch between the HI and LI to the drivers for both the falling and rising thresholds ensures dead times of < 10 ns. Co-packaging the GaN FET half-bridge with the driver ensures minimized common source inductance. This minimized inductance has a significant performance impact on hard-switched topologies.

The built-in bootstrap circuit with clamp prevents the high-side gate drive from exceeding the GaN FETs maximum gate-to-source voltage (Vgs) without any additional external circuitry. The built-in driver has an undervoltage lockout (UVLO) on the VDD and bootstrap (HB-HS) rails. When the voltage is below the UVLO threshold voltage, the device ignores both the HI and LI signals to prevent the GaN FETs from being partially turned on. Below UVLO, if there is sufficient voltage (V_{VCC} > 2.5 V), the driver actively pulls the high-side and low-side gate driver output low. The UVLO threshold hysteresis of 200 mV prevents chattering and unwanted turnon due to voltage spikes. Use an external VCC bypass capacitor with a value of 0.1 µF or higher. TI recommends a size of 0402 to minimize trace length to the pin. Place the bypass and bootstrap capacitors as close as possible to the device to minimize parasitic inductance.

9.3.1 Control Inputs

The LMG2100R044's inputs pins are independently controlled with TTL input thresholds and can withstand voltages up to 12V regardless of the VDD voltage. This allows the inputs to be directly connected to the outputs of an analog PWM controller with up to 12V power supply, eliminating the need for a buffer stage.

In order to allow flexibility to optimize deadtime according to design needs, the LMG2100R044 does not implement an overlap protection functionality. If both HI and LI are asserted, both the high-side and low-side GaN FETs are turned on. Careful consideration must be applied to the control inputs in order to avoid a shoot-through condition.

9.3.2 Start-up and UVLO

The LMG2100R044 has an UVLO on both the V_{CC} and HB (bootstrap) supplies. When the V_{CC} voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also, if there is insufficient V_{CC} voltage, the UVLO actively pulls the high- and low-side GaN FET gates low. When the HB to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only the high-side GaN FET gate is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

Table 9-1. V_{CC} UVLO Feature Logic Operation

CONDITION (V_{HB-HS} > V_{HBR} for all cases below)	HI	LI	SW
V_{CC} - V_{SS} < V_{CCR} during device start-up	H	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	L	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	H	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	L	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	H	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	L	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	H	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	L	L	Hi-Z

Table 9-2. V_{HB-HS} UVLO Feature Logic Operation

CONDITION (V_{CC} > V_{CCR} for all cases below)	HI	LI	SW
V_{HB-HS} < V_{HBR} during device start-up	H	L	Hi-Z
V_{HB-HS} < V_{HBR} during device start-up	L	H	PGND
V_{HB-HS} < V_{HBR} during device start-up	H	H	PGND

Table 9-2. V_{HB-HS} UVLO Feature Logic Operation (continued)

CONDITION (V_{CC} > V_{CCR} for all cases below)	HI	LI	SW
V_{HB-HS} < V_{HBR} during device start-up	L	L	Hi-Z
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	H	L	Hi-Z
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	L	H	PGND
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	H	H	PGND
V_{HB-HS} < V_{HBR} - $V_{HB(hyst)}$ after device start-up	L	L	Hi-Z

9.3.3 Bootstrap Supply Voltage Clamping

The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5 V (typical). This clamp prevents the gate voltage from exceeding the maximum gate-source voltage rating of the enhancement-mode GaN FETs.

9.3.4 Level Shift

The level-shift circuit is the interface from the high-side input HI to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the high-side GaN FET gate driver output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

ADVANCE INFORMATION

9.4 Device Functional Modes

The LMG2100R044 operates in normal mode and UVLO mode. See *Section 9.3.2* for information on UVLO operation mode. In the normal mode, the output state is dependent on the states of the HI and LI pins. Table 9-3 lists the output states for different input pin combinations. Note that when both HI and LI are asserted, both GaN FETs in the power stage are turned on. Careful consideration must be applied to the control inputs in order to avoid this state, as it will result in a shoot-through condition, which can permanently damage the device.

Table 9-3. Truth Table

HI	LI	HIGH-SIDE GaN FET	LOW-SIDE GaN FET	SW
L	L	OFF	OFF	Hi-Z
L	H	OFF	ON	PGND
H	L	ON	OFF	VIN
H	H	ON	ON	- - -

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LMG2100R044 GaN power stage is a versatile building block for various types of high-frequency, switch-mode power applications. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the GaN FETs. The device design is highly optimized for synchronous buck converters and other half-bridge configurations.

10.2 Typical Application

Figure 10-1 shows a synchronous buck converter application with V_{CC} connected to a 5-V supply. It is critical to optimize the power loop (loop impedance from VIN capacitor to PGND). Having a high power loop inductance causes significant ringing in the SW node and also causes the associated power loss. The LMG2100R044 has VIN and PGND pins next to each other. This enables the VIN capacitor to be placed very close to LMG2100R044 on the top layer of the PCB, minimizing power loop inductance.

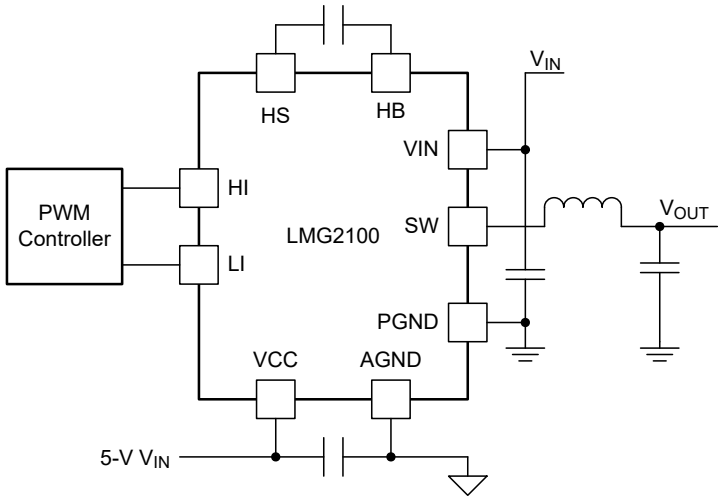

Figure 10-1. Typical Connection Diagram For a Synchronous Buck Converter

ADVANCE INFORMATION

10.2.1 Design Requirements

When designing a synchronous buck converter application that incorporates the LMG2100R044 power stage, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are the input voltages, passive components, operating frequency, and controller selection. *Table 10-1* shows some sample values for a typical application. See *Section 10.3*, *Section 10.4*, and *Section 10.2.2.3* for other key design considerations for the LMG2100R044.

Table 10-1. Design Parameters

PARAMETER	SAMPLE VALUE
Half-bridge input supply voltage, V_{IN}	48 V
Output voltage, V_{OUT}	12 V
Output current	8 A
V_{HB-HS} bootstrap capacitor	0.1 uF, X5R
Switching frequency	1 MHz
Dead time	8 ns
Inductor	4.7 µH
Controller	LM5148

10.2.2 Detailed Design Procedure

This procedure outlines the design considerations of LMG2100R044 in a synchronous buck converter. For additional design help, see *Section 11.2.1*.

10.2.2.1 V_{CC} Bypass Capacitor

The V_{CC} bypass capacitor provides the gate charge for the low-side and high-side transistors and to absorb the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with Equation 1.

$$C_{VCC} = (Q_{gH} + Q_{gL} + Q_{rr}) / \Delta V \quad (1)$$

Q_{gH} and Q_{gL} are the gate charge of the high-side and low-side transistors, respectively. Q_{rr} is the reverse recovery charge of the bootstrap diode. ΔV is the maximum allowable voltage drop across the bypass capacitor. A 0.1-µF or larger value, good-quality, ceramic capacitor is recommended. Place the bypass capacitor as close as possible to the V_{CC} and AGND pins of the device to minimize the parasitic inductance.

10.2.2.2 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side gate drive, dc bias power for HB UVLO circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated using Equation 2.

$$C_{BST} = (Q_{gH} + Q_{rr} + I_{HB} * t_{ON(max)}) / \Delta V \quad (2)$$

where

- I_{HB} is the quiescent current of the high-side gate driver (150 µA, maximum)
- t_{ON}(maximum) is the maximum on-time period of the high-side gate driver
- Q_{rr} is the reverse recovery charge of the bootstrap diode
- Q_{gH} is the gate charge of the high-side GaN FET
- ΔV is the permissible ripple in the bootstrap capacitor (< 100 mV, typical)

A 0.1-µF, 16-V, 0402 ceramic capacitor is suitable for most applications. Place the bootstrap capacitor as close as possible to the HB and HS pins.

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10.2.2.3 Power Dissipation

Ensure that the power loss in the driver and the GaN FETs is maintained below the maximum power dissipation limit of the package at the operating temperature. The smaller the power loss in the driver and the GaN FETs, the higher the maximum operating frequency that can be achieved in the application. The total power dissipation of the LMG2100R044 device is the sum of the gate driver losses, the bootstrap diode power loss and the switching and conduction losses in the FETs.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated using Equation 3.

$$P = (2 \times Q_g) \times V_{DD} \times f_{SW} \quad (3)$$

where

- Q_g is the gate charge
- V_{DD} is the bias supply
- f_{SW} is the switching frequency

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the outputs.

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Because each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

The power losses due to the GaN FETs can be divided into conduction losses and switching losses. Conduction losses are resistive losses and can be calculated using Equation 4.

$$P_{COND} = \left[(I_{RMS(HS)})^2 \times RDS_{(on)HS} \right] + \left[(I_{RMS(LS)})^2 \times RDS_{(on)LS} \right] \quad (4)$$

where

- $R_{DS(on)HS}$ is the high-side GaN FET on-resistance
- $R_{DS(on)LS}$ is the low-side GaN FET on-resistance
- $I_{RMS(HS)}$ is the high-side GaN FET RMS current
- $I_{RMS(LS)}$ and low-side GaN FET RMS current

The switching losses can be computed to a first order using , t_{TR} can be approximated by dividing V_{IN} by 25V/ns, which is a conservative estimate of the switched node slew rate. Equation 5.

$$P_{SW} = V_{IN} \times I_{OUT} \times f_{SW} \times t_{TR} \quad (5)$$

where

- t_{TR} is the switch transition time from ON to OFF and from OFF to ON

Note that the low-side FET does not suffer from this loss. The third quadrant loss in the low-side device is ignored in this first order loss calculation.

As described previously, switching frequency has a direct effect on device power dissipation. Although the gate driver of the LMG2100R044 device is capable of driving the GaN FETs at frequencies up to 10 MHz, careful consideration must be applied to ensure that the running conditions for the device meet the recommended operating temperature specification. Specifically, hard-switched topologies tend to generate more losses and self-heating than soft-switched applications.

The sum of the driver loss, the bootstrap diode loss, and the switching and conduction losses in the GaN FETs is the total power loss of the device. Careful board layout with an adequate amount of thermal vias close to the power pads (VIN and PGND) allows optimum power dissipation from the package. A top-side mounted heat sink with airflow can also improve the package power dissipation.

10.3 Power Supply Recommendations

The recommended bias supply voltage range for LMG2100R044 is from 4.75 V to 5.25 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the V_{CC} supply circuit. The upper end of this range is driven by the 6 V absolute maximum voltage rating of V_{CC}. Note that the gate voltage of the low-side GaN FET is not clamped internally. Hence, it is important to keep the V_{CC} bias supply within the recommended operating range to prevent exceeding the low-side GaN transistor gate breakdown voltage.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{CC} voltage drops, the device continues to operate in normal mode as far as the voltage drop does not exceeds the hysteresis specification, $V_{CC(hyst)}$. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LMG2100R044 to avoid triggering device-shutdown.

Place a local bypass capacitor between the VDD and VSS pins. This capacitor must be located as close as possible to the device. A low ESR, ceramic surface-mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

10.4 Layout

10.4.1 Layout Guidelines

To maximize the efficiency benefits of fast switching, it is extremely important to optimize the board layout such that the power loop impedance is minimal. When using a multilayer board (more than 2 layers), power loop parasitic impedance is minimized by having the return path to the input capacitor (between VIN and PGND), small and directly underneath the first layer as shown in Figure 10-2 and Figure 10-3. Loop inductance is reduced due to flux cancellation as the return current is directly underneath and flowing in the opposite direction. It is also critical that the VCC capacitors and the bootstrap capacitors are as close as possible to the device and in the first layer. Carefully consider the AGND connection of LMG2100R044 device. It must NOT be directly connected to PGND so that PGND noise does not directly shift AGND and cause spurious switching events due to noise injected in HI and LI signals.

10.4.2 Layout Examples

Placements shown in Figure 10-2 and in the cross section of Figure 10-3 show the suggested placement of the device with respect to sensitive passive components, such as VIN, bootstrap capacitors (HS and HB) and VSS capacitors. Use appropriate spacing in the layout to reduce creepage and maintain clearance requirements in accordance with the application pollution level. Inner layers if present can be more closely spaced due to negligible pollution.

The layout must be designed to minimize the capacitance at the SW node. Use as small an area of copper as possible to connect the device SW pin to the inductor, or transformer, or other output load. Furthermore, ensure that the ground plane or any other copper plane has a cutout so that there is no overlap with the SW node, as this would effectively form a capacitor on the printed circuit board. Additional capacitance on this node reduces the advantages of the advanced packaging approach of the LMG2100R044 and may result in reduced performance.

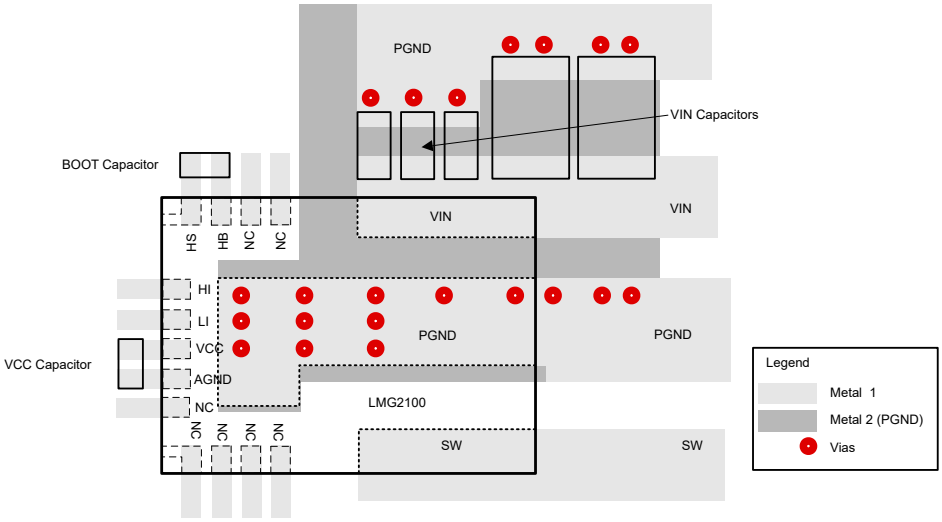

Figure 10-2. External Component Placement (Multi-layer PCB)

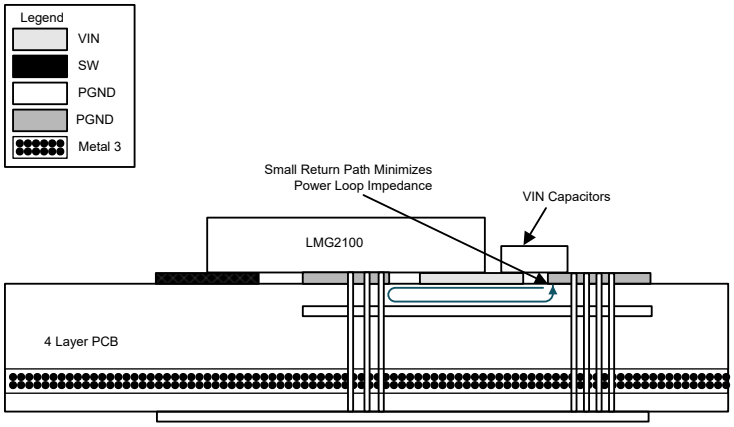

Figure 10-3. Four-Layer Board Cross Section With Return Path Directly Underneath for Power Loop

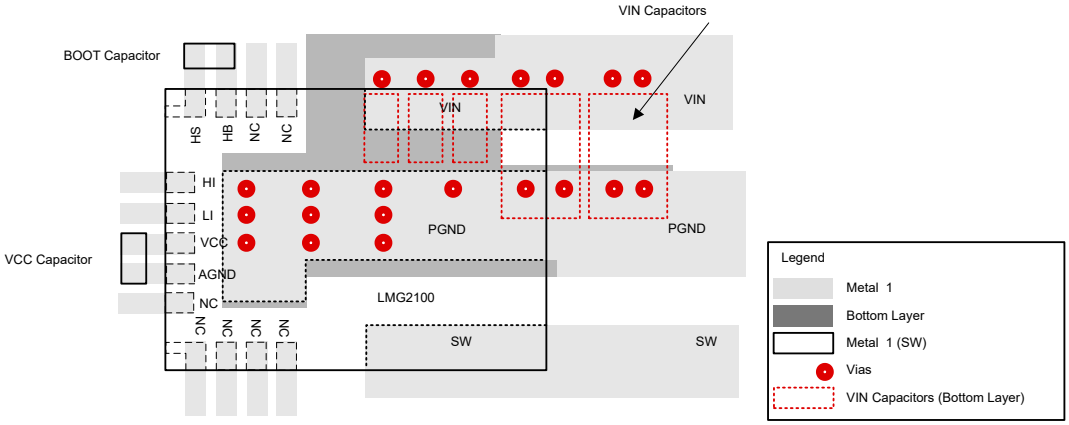

Figure 10-4. External Component Placement (Double Layer PCB)

ADVANCE INFORMATION

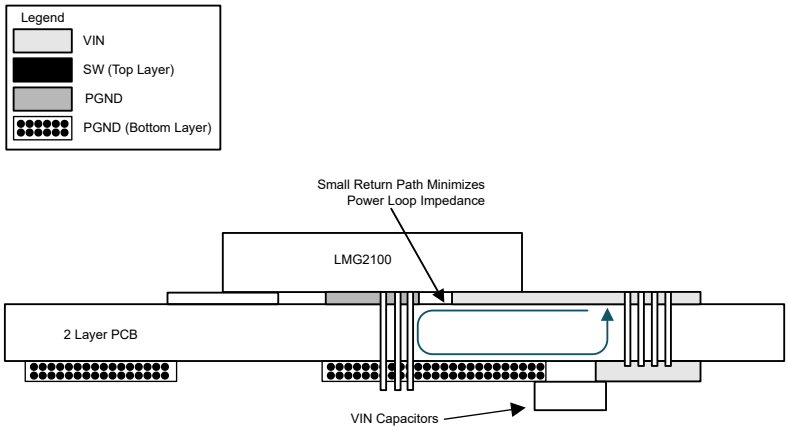

Figure 10-5. Two-Layer Board Cross Section With Return Path

Two-layer boards are not recommended for use with LMG2100R044 device due to the larger power loop inductance. However, if design considerations allow only two board layers, place the input decoupling capacitors immediately behind the device on the back-side of the board to minimize loop inductance. Figure 10-4 and Figure 10-5 show a layout example for two-layer boards.

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.2 Documentation Support

11.2.1 Related Documentation

Layout Guidelines for LMG2100R044 GaN Power Stage Module

Using the LMG2100R044: GaN Half-Bridge Power Module Evaluation Module

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

11.5 Trademarks

All trademarks are the property of their respective owners.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Information

The LMG2100R044 device package is rated as an MSL3 package (Moisture Sensitivity Level 3). Refer to application report *AN-2029 Handling and Process Recommendations* for specific handling and process recommendations of an MSL3 package.

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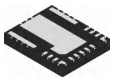
ADVANCE INFORMATION

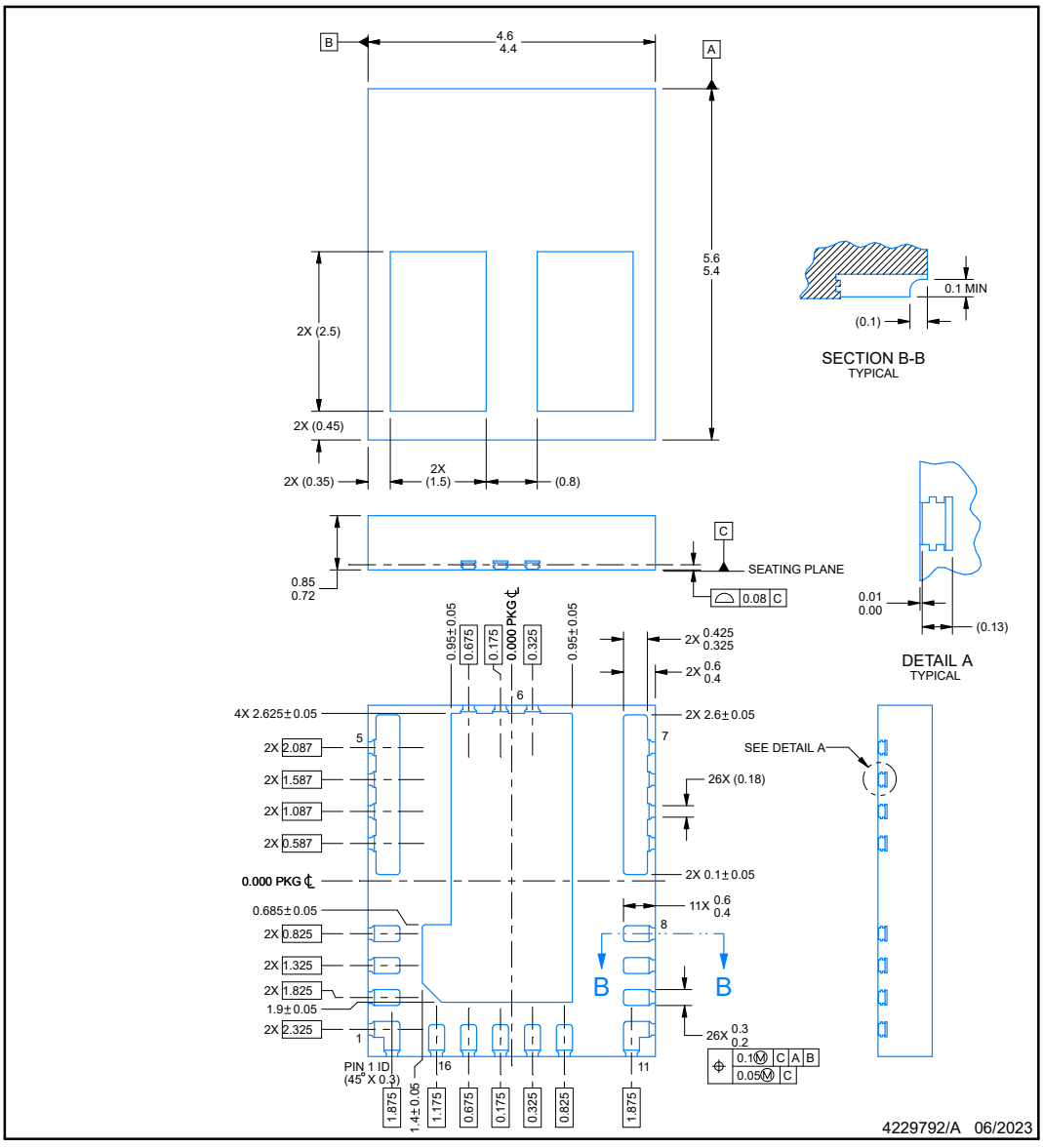
PACKAGE OUTLINE

RAR0016A-C01



VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



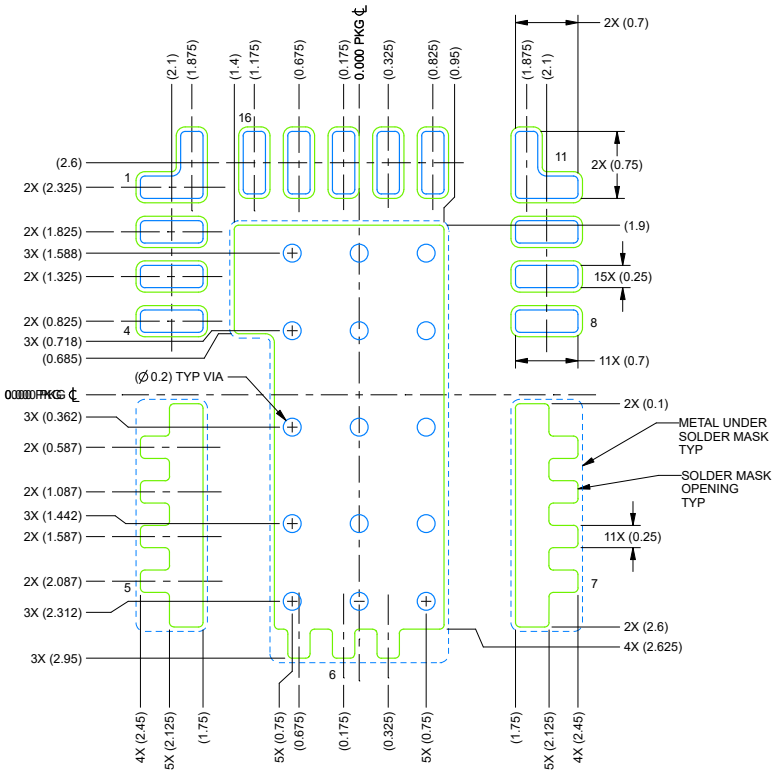
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

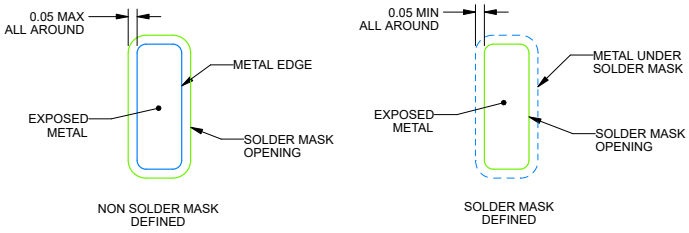
EXAMPLE BOARD LAYOUT

RAR0016A-C01 — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

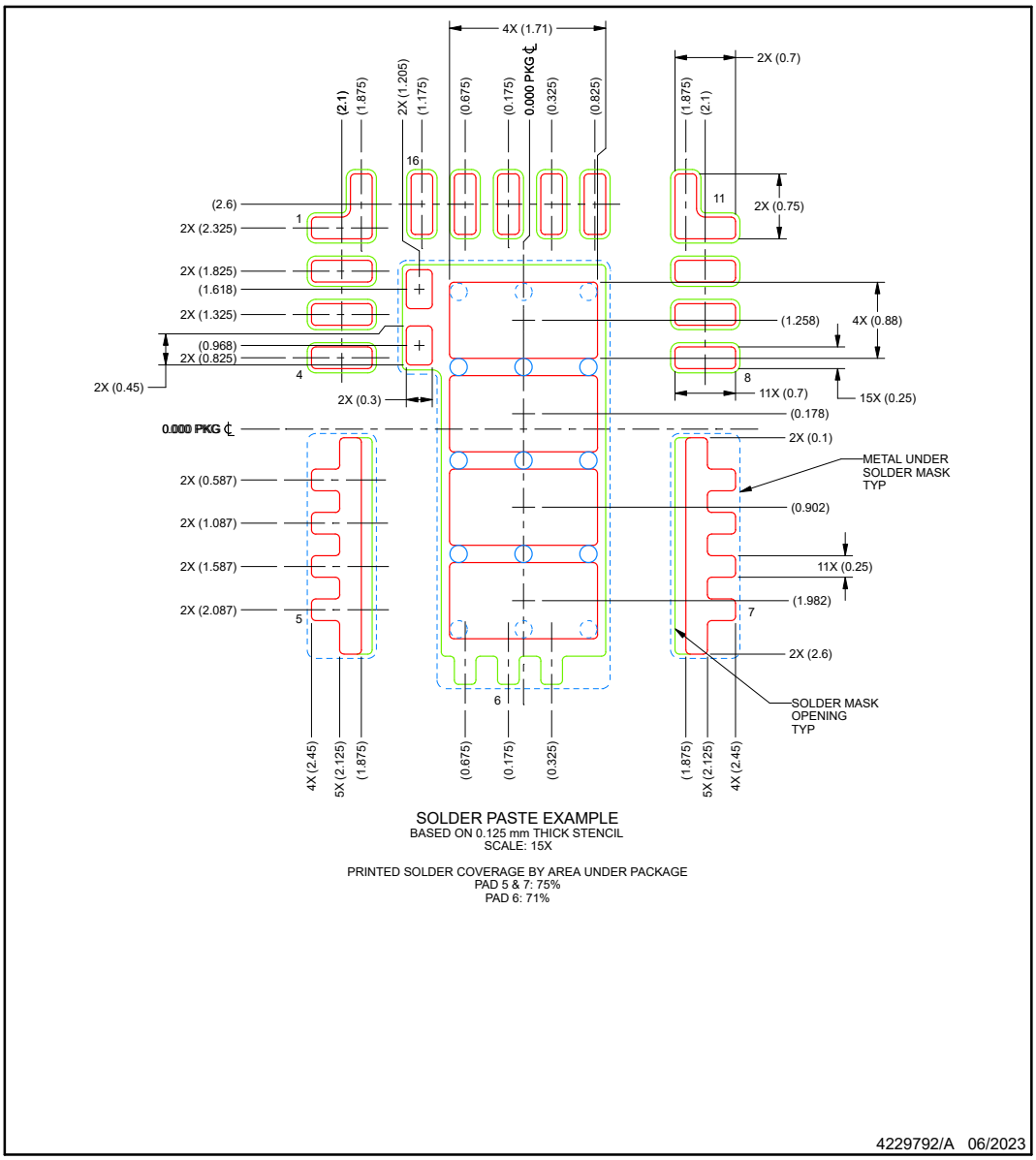
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RAR0016A-C01 — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 5 & 7: 75%
PAD 6: 71%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XLMG2100R044RARR	ACTIVE	VQFN-FCRLF	RAR	16	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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