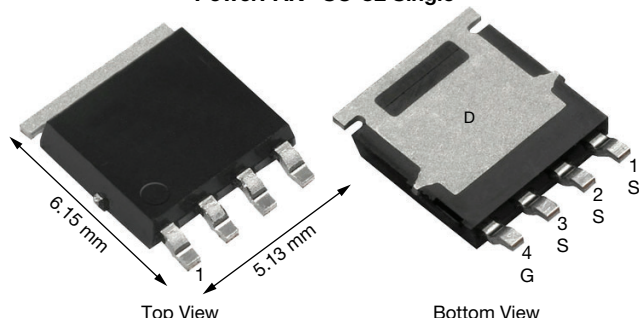
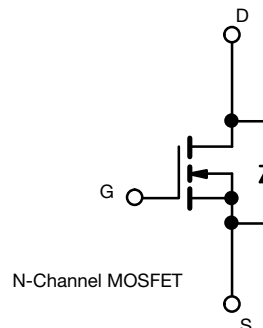


Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Single


FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0024
I_D (A)	75
Configuration	Single
Package	PowerPAK SO-8L

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	$T_C = 25$ °C ^a	I_D	75	A
	$T_C = 125$ °C		65.6	
Continuous source current (diode conduction)		I_S	62	
Pulsed drain current ^b		I_{DM}	200	
Single pulse avalanche current	$L = 0.1$ mH	I_{AS}	44	mJ
		E_{AS}	96.8	
Maximum power dissipation ^b	$T_C = 25$ °C	P_D	68	W
	$T_C = 125$ °C		22	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^c	R_{thJA}	68	°C/W
Junction-to-case (drain)		R_{thJC}	2.2	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	3.0	3.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	200	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.0020	0.0024	Ω
		V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.0040	
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0050	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 10 A		-	48	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	4005	5250	pF
Output capacitance	C _{oss}			-	1160	1550	
Reverse transfer capacitance	C _{rss}			-	90	120	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 10 A	-	66	100	nC
Gate-source charge ^c	Q _{gs}			-	17	-	
Gate-drain charge ^c	Q _{gd}			-	14	-	
Gate resistance	R _g	f = 1 MHz		0.35	0.76	1.2	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		-	17	30	ns
Rise time ^c	t _r			-	17	30	
Turn-off delay time ^c	t _{d(off)}			-	32	50	
Fall time ^c	t _f			-	8	15	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	200	A
Forward voltage	V _{SD}	I _F = 10 A, V _{GS} = 0 V		-	0.76	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs		-	65	130	ns
Body diode reverse recovery charge	Q _{rr}			-	123	250	nC
Reverse recovery fall time	t _a			-	35	-	ns
Reverse recovery rise time	t _b			-	30	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			-	-3.3	-	A

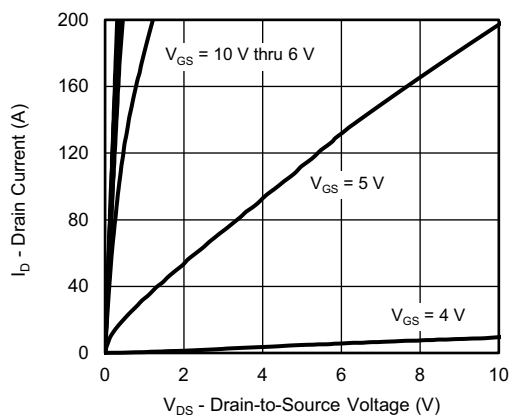
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

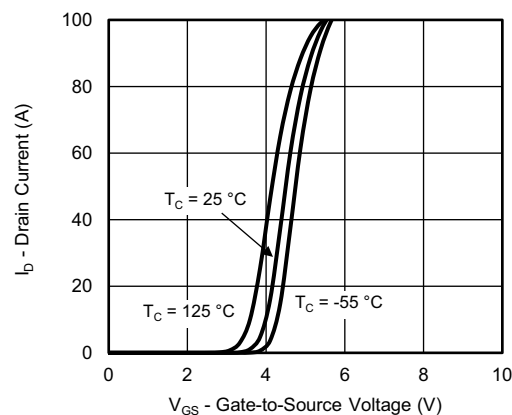
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



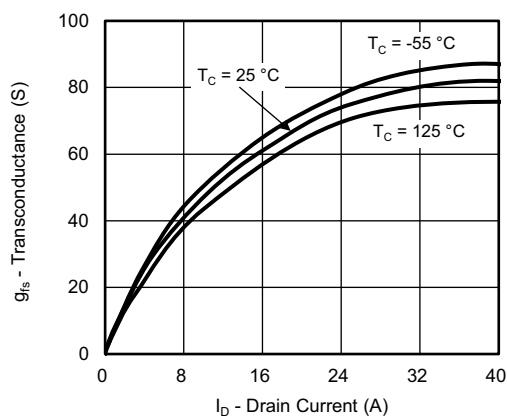
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



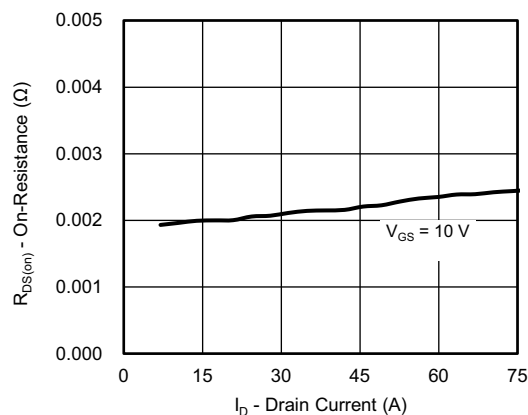
Output Characteristics



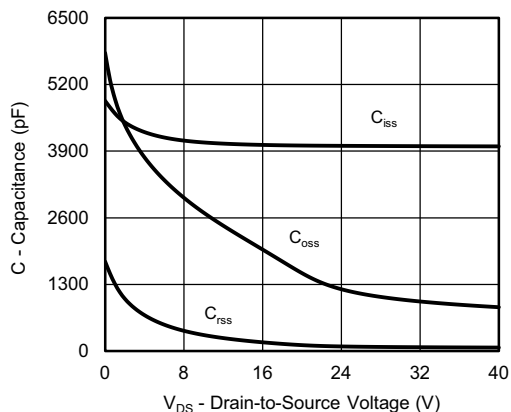
Transfer Characteristics



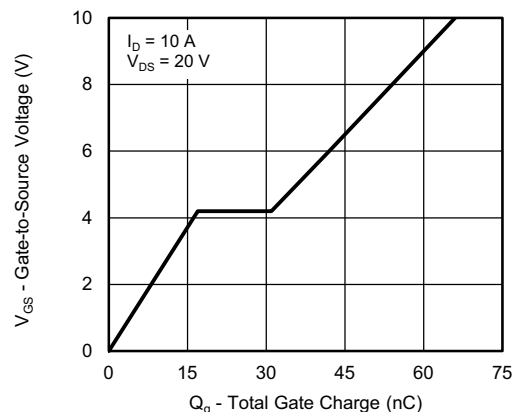
Transconductance



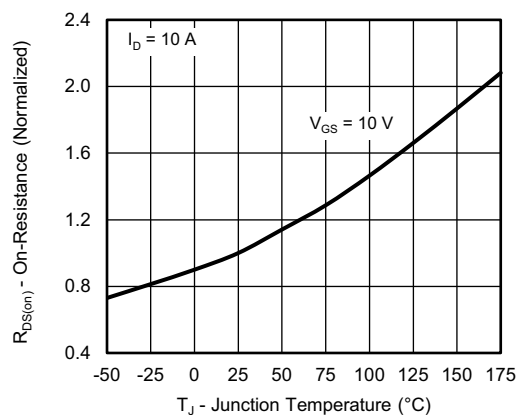
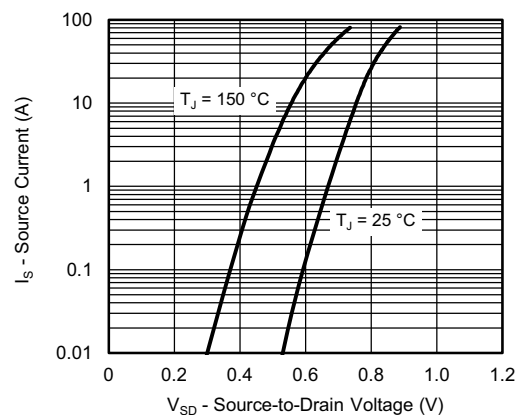
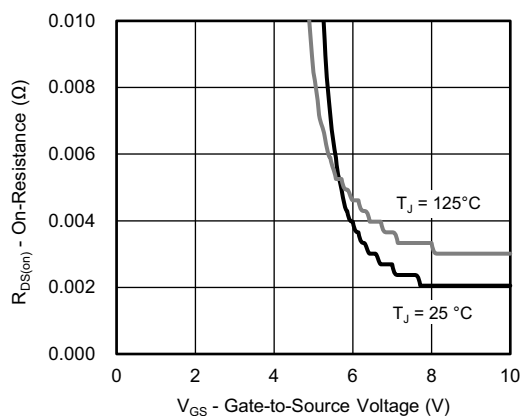
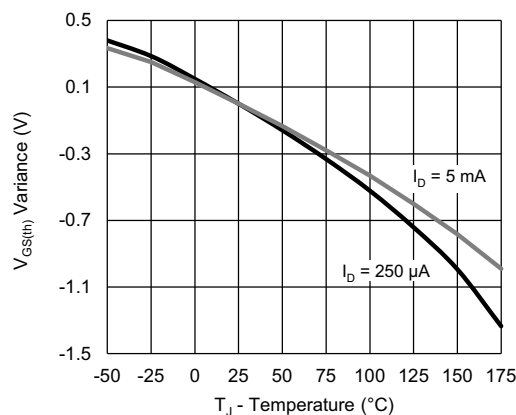
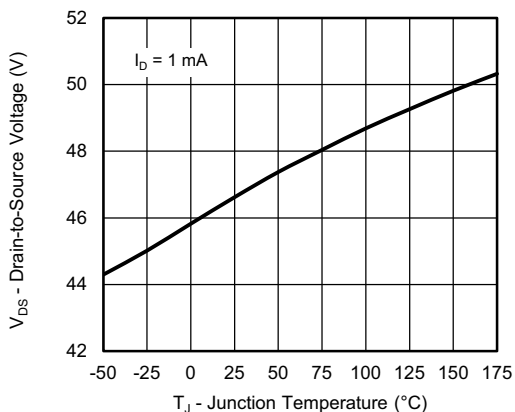
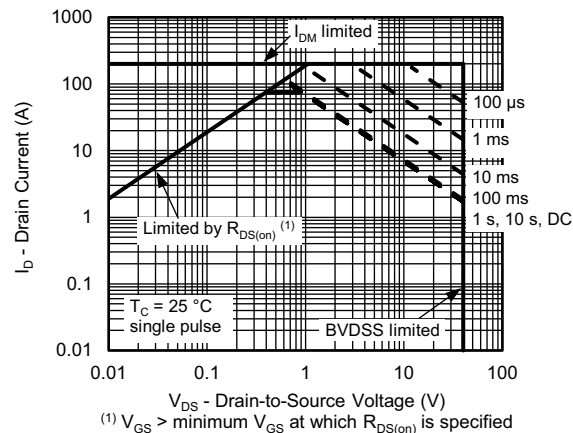
On-Resistance vs. Drain Current

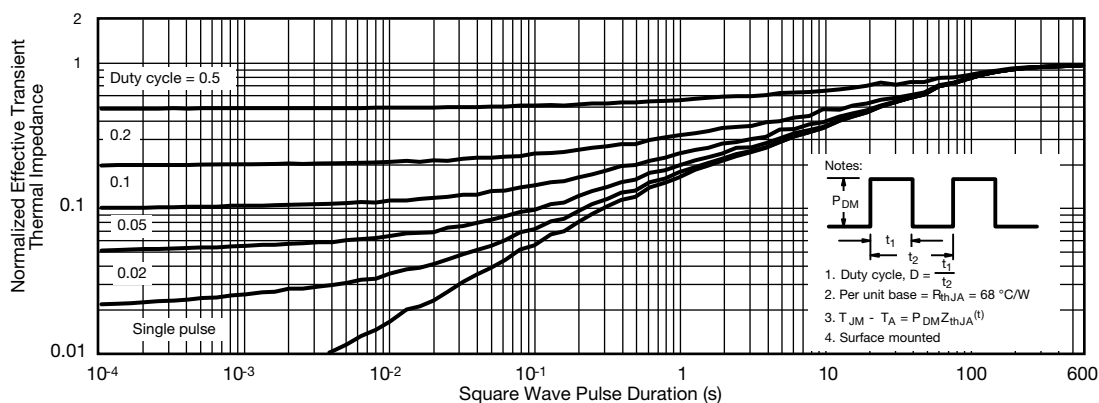
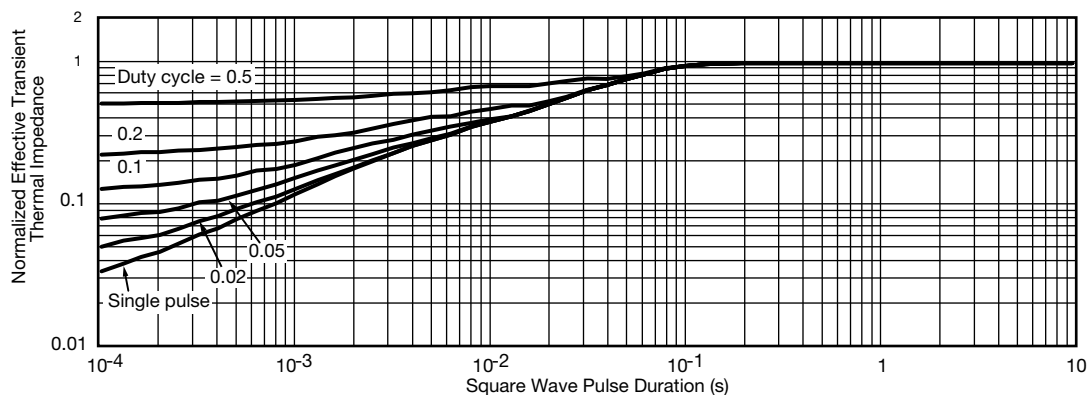


Capacitance



Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

Safe Operating Area

**TYPICAL CHARACTERISTICS** ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case****Note**

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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